A Novel Variation-Aware Low-Power Keeper Architecture for Wide Fan-in Dynamic Gates

ECE 225
Lecture 15

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Outline

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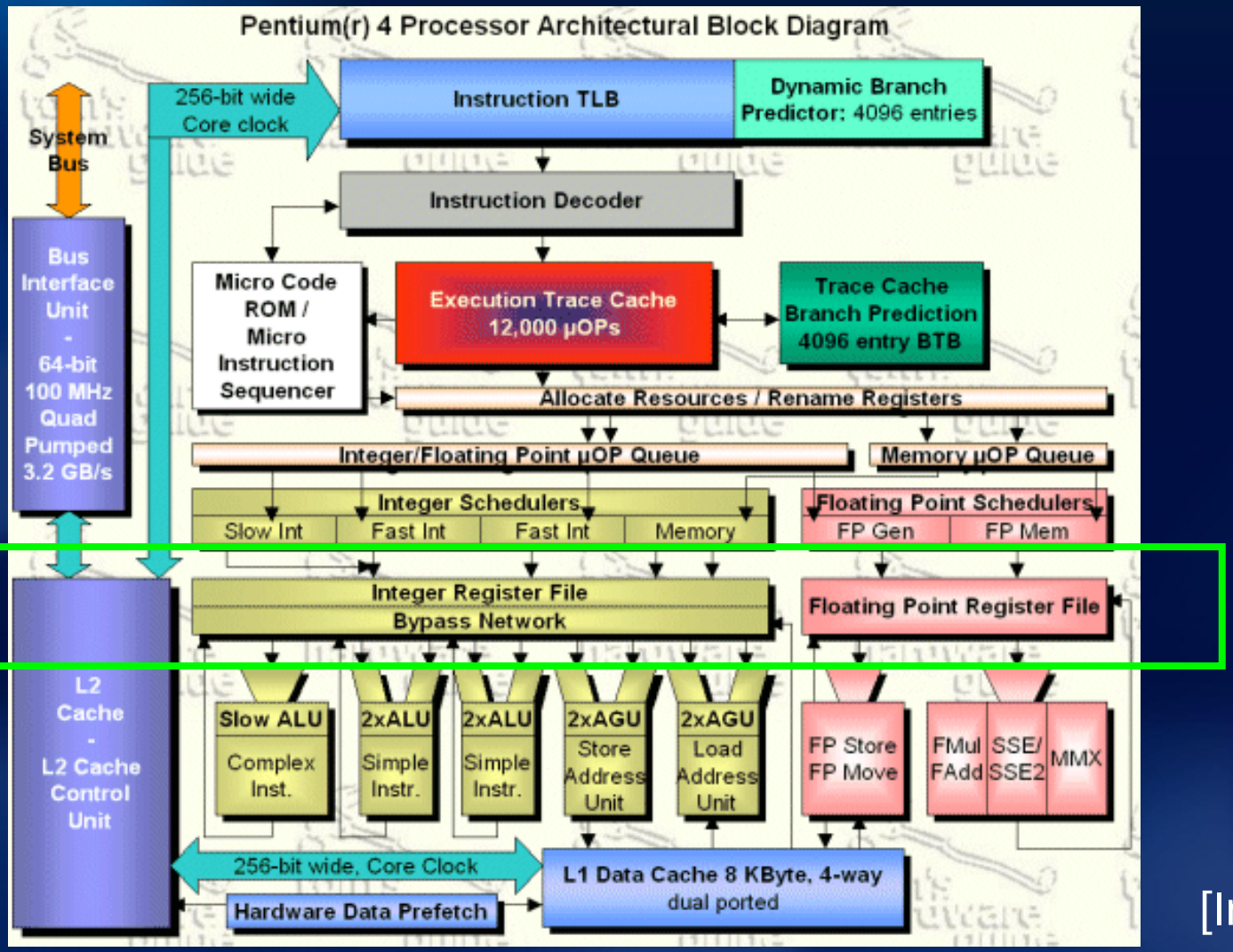
- Introduction
- Process Variation
- Keeper Sizing
- Proposed Keeper
- Implementation and Results
- Conclusions

Motivation



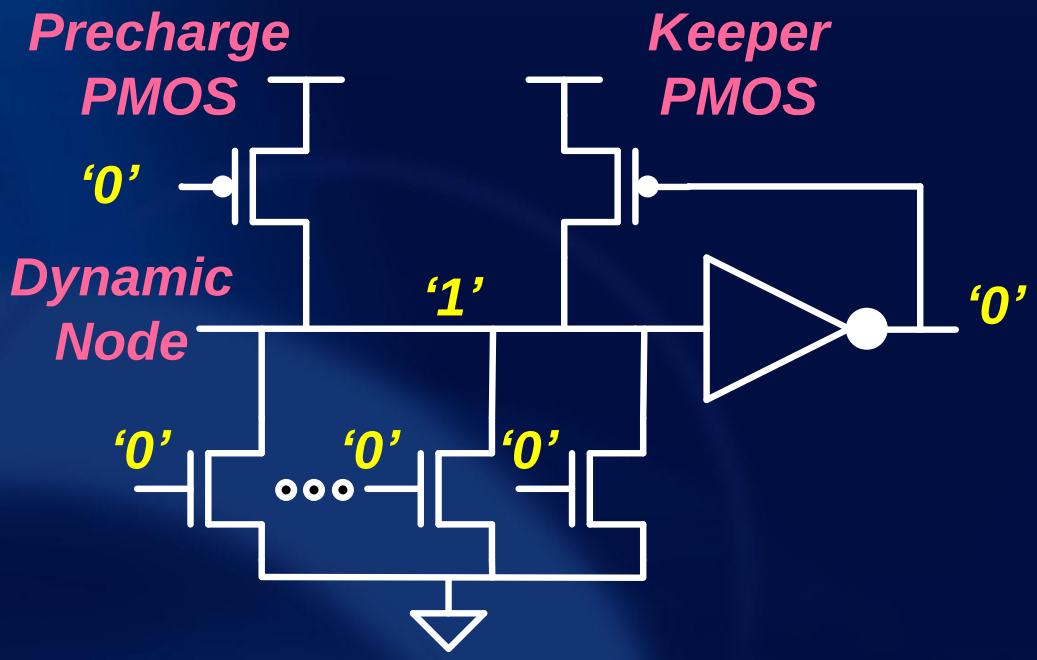
[Intel Inc.]

- **Register files are critical modules in computer architecture**

Motivation

- Register files are one of the most important components of modern micro-processors.
- Since dynamic gates offer high performance, register files are realized using this type of gate style.
- Wide-Fan-In dynamic OR gates are widely employed in different parts of a register file, such as address decoder and multiplexers.
- Improving performance of wide-Fan-In dynamic OR can significantly improve performance of register files and micro-processors consequently.

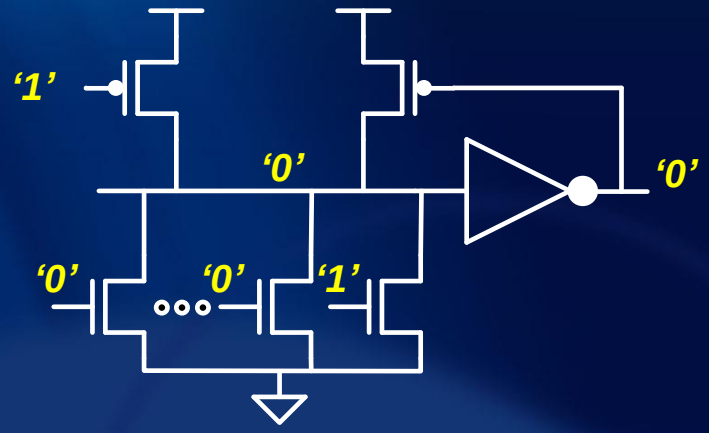
Introduction



Precharge Phase

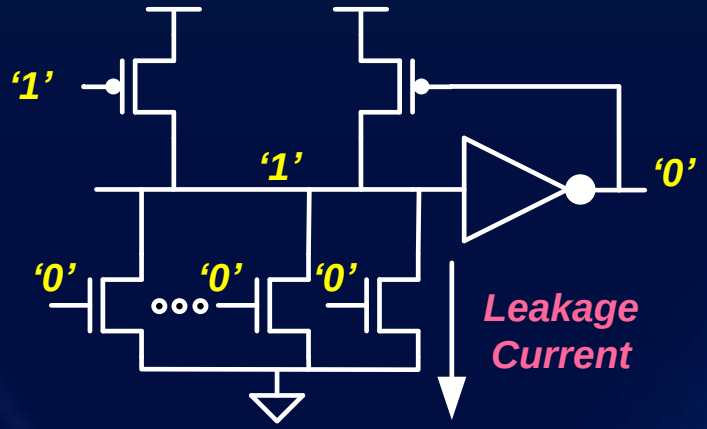
- **Pre-charge phase for a wide dynamic OR gate**

Introduction



(a) Evaluation Phase :

Larger keeper makes it tougher for NMOS to pull down the dynamic node.

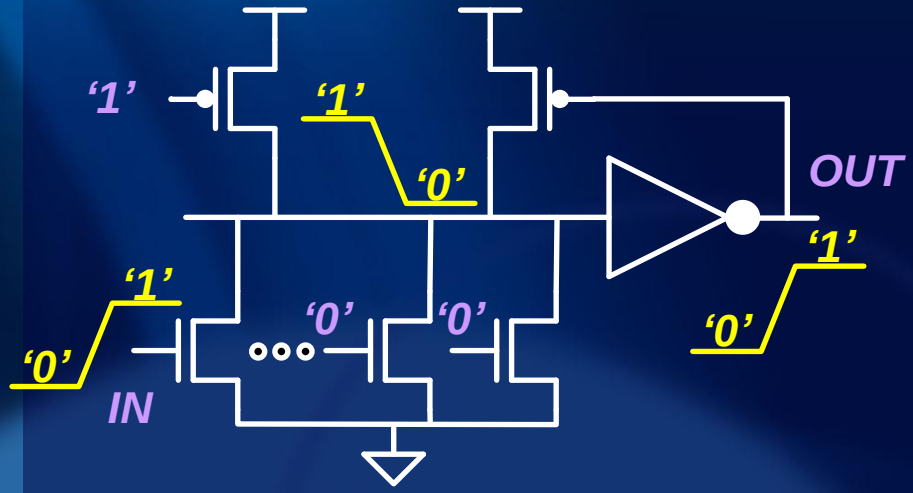


(b) Evaluation Phase :

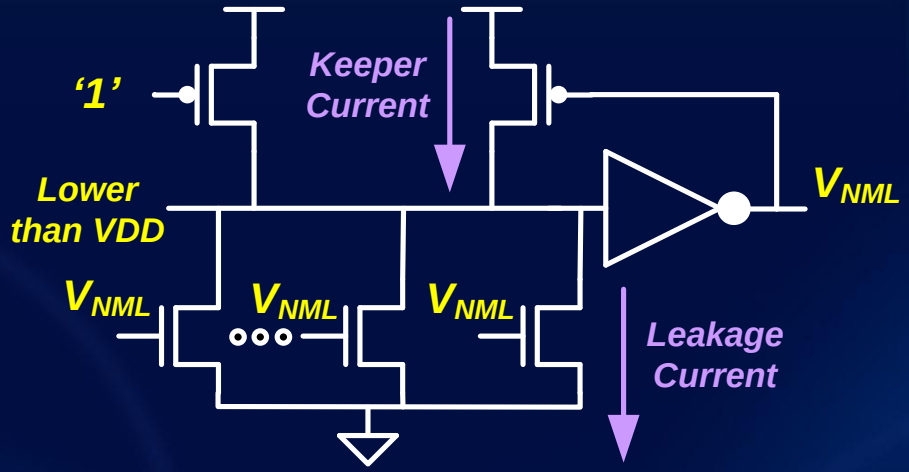
Larger keeper is required to maintain the high voltage of the dynamic node.

- **Trade-off between performance and robustness.**
- **Delay is calculated when only one input in high.**
- **Noise margin, on the other hand, is measured when all inputs are low.**

Introduction



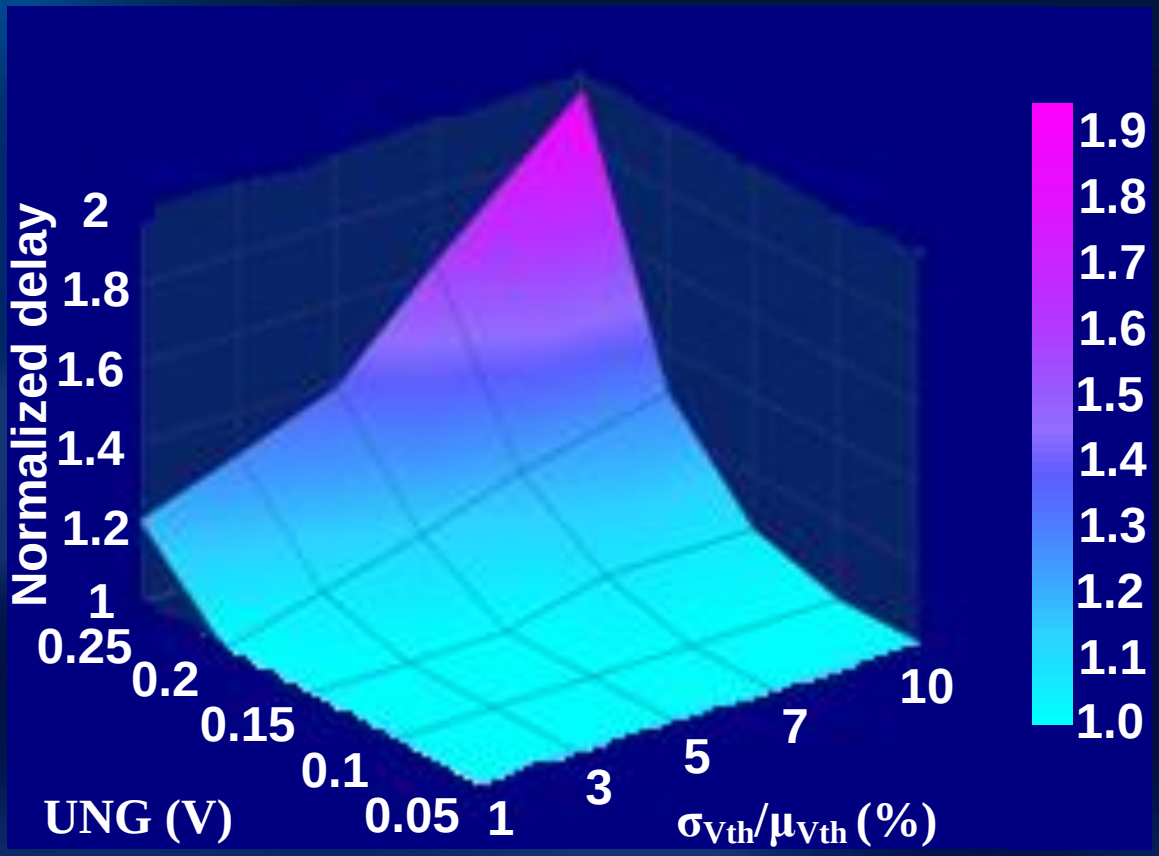
Delay of dynamic gate



Noise margin (Unity Noise Gain)

- Worst case delay is measured when only one input switches (delay from IN to OUT node).
- Noise margin is measured in Unity Gain Margin (UNG) that is the voltage level that when applied to all inputs, results in equal output node voltage.

Introduction

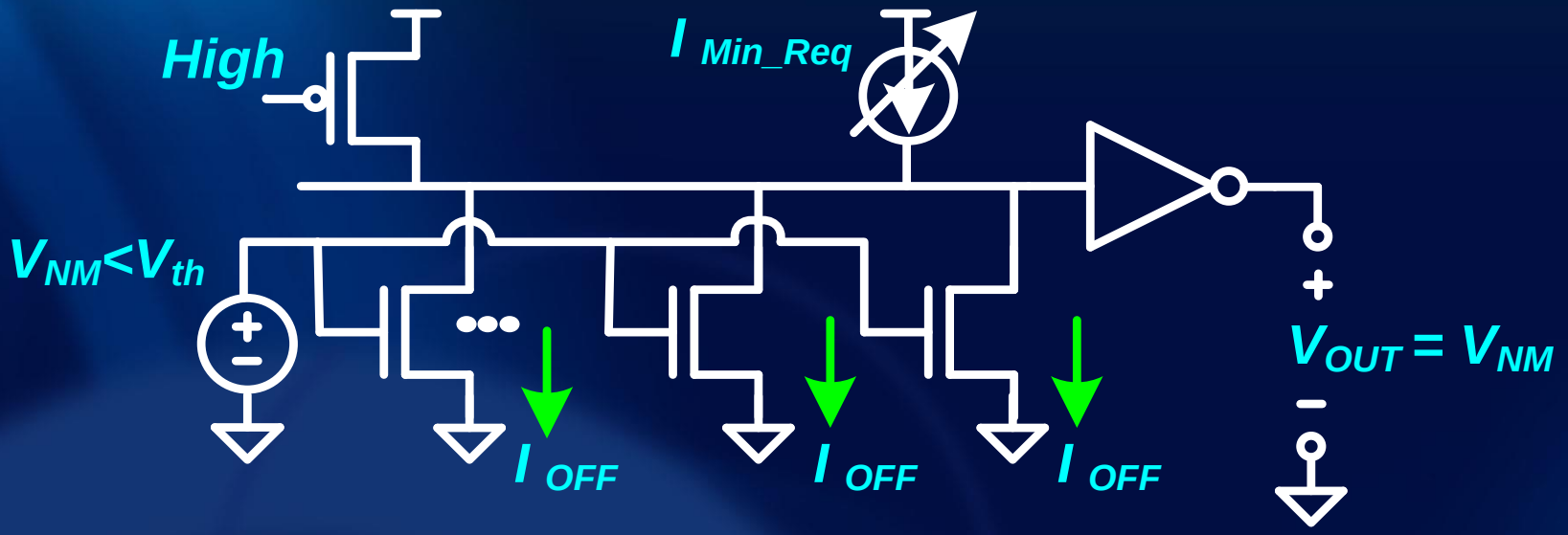


- **Graphical presentation of trade-off between delay and noise margin of a wide dynamic OR gate under process variation.**

Process Variation

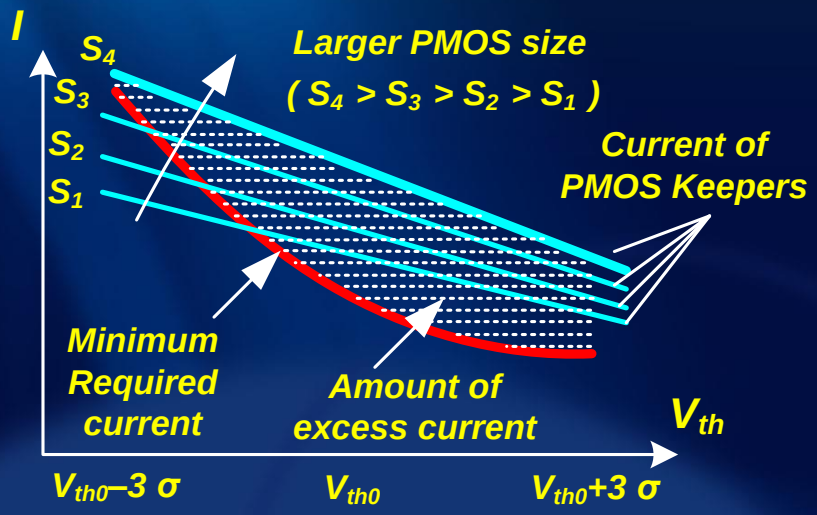
- In this work we focus on correlated variation of threshold voltage; it means that we assume V_{th} of all transistors in a single dynamic gate are altered in same way.
- Impact of random variation can be considered by targeting an appropriate higher design margins.

Keeper Sizing

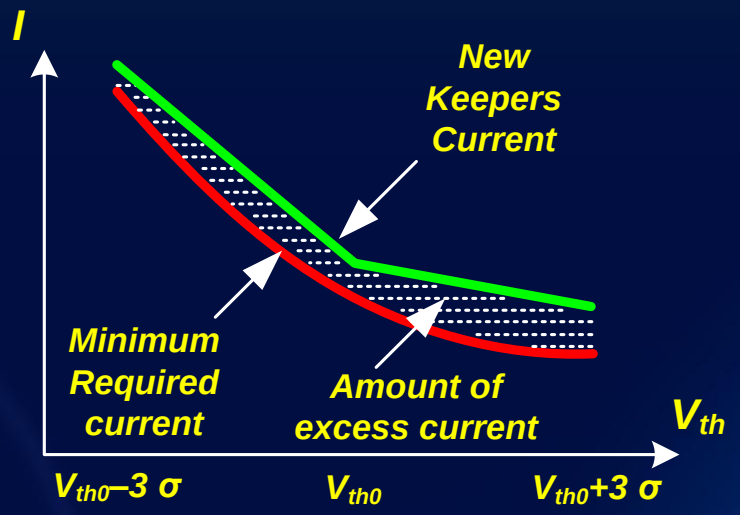


- Minimum required current: Is defined as smallest amount of current that must be injected to dynamic node to guarantee an specified level of UNG.
- Minimum required current will vary as process variation changes V_{th} of pull down network transistors.
- Circuit configuration for measuring UNG under process variation is shown here.

Keeper Sizing



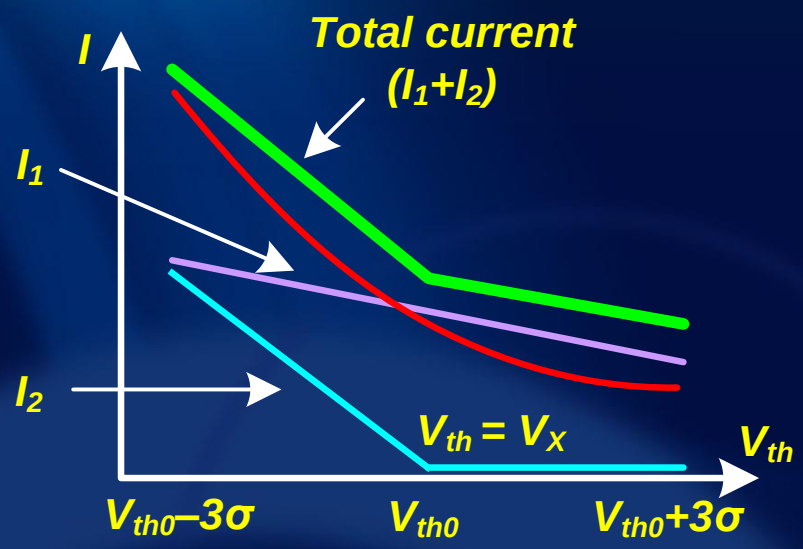
(a) Traditional keeper's behavior

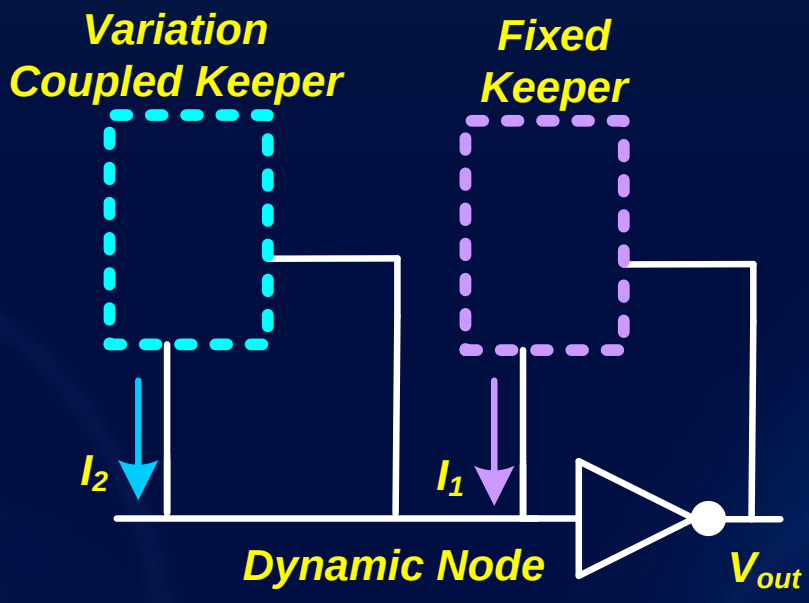


(b) Proposed keeper's behavior

- To maintain the minimum required current level over entire variation range, traditional PMOS keeper must be resized.
- At lower threshold voltage, top line (S_4) supplies enough current; however, at higher threshold voltage huge amount of excess current is injected to node.

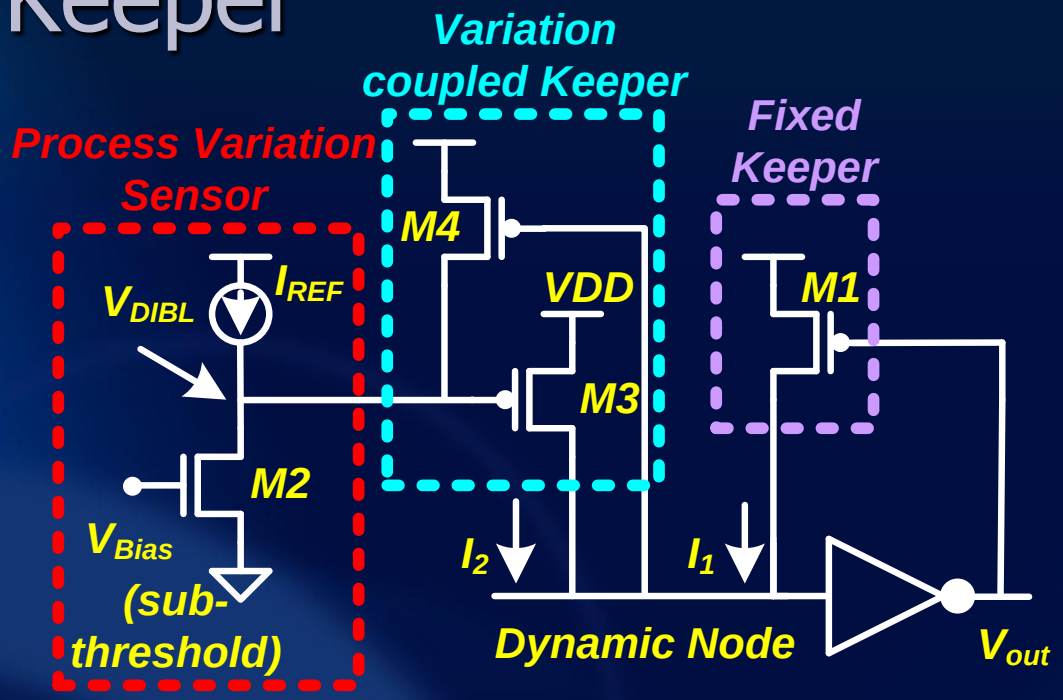
Proposed Keeper





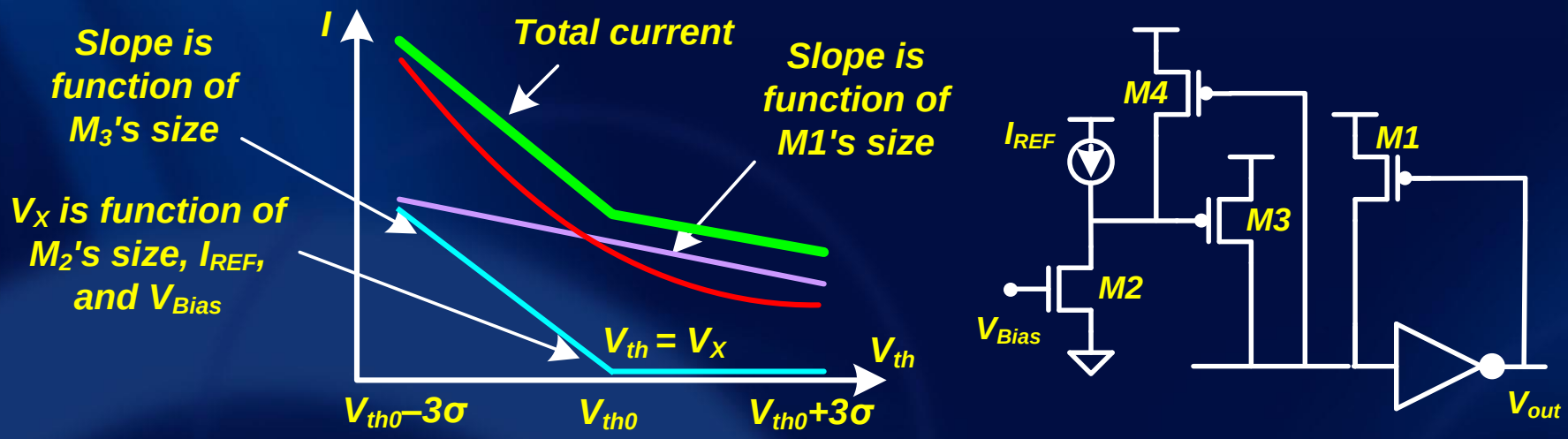
- New keeper is composed of two circuits.
- First one is a small fixed-size PMOS keeper.
- Second one is a variation-coupled keeper.
- Total current shows much better behavior compared to traditional PMOS keepers.

Proposed Keeper



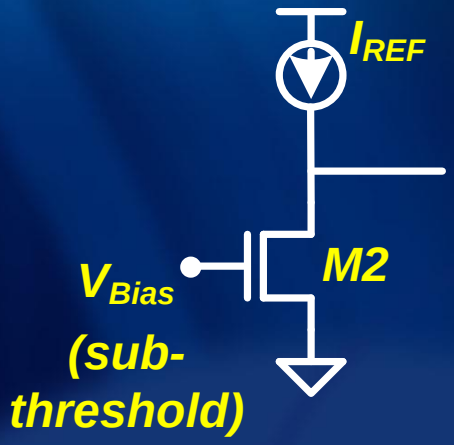
- Beside two keepers, there is a process variation sensor.
- On lower V_{th} side, variation sensor provides higher V_{DIBL} voltage and hence, M_3 supplies less current. On higher V_{th} side vice versa.
- M4 is used to turn off M3 keeper when dynamic node needs to be pulled down.

Proposed Keeper



- **Through analytical equations, circuit parameter affecting keeper current curves have been studied.**
- **It is shown that each circuit parameter affects a separate part of curves which gives more flexibility in adjusting current curves to get best possible results.**

Proposed Keeper



Process Variation Sensor (Kuroda et al. ISSCC 1996)

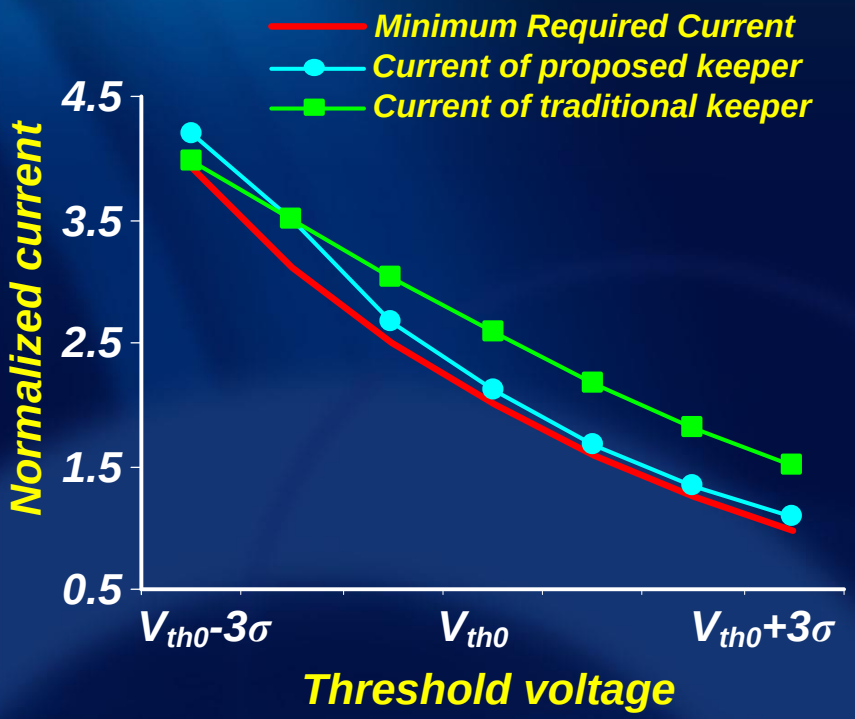
(a) $I_{REF} = \mu_n C_{ox} \frac{W}{L} V_T^{\,2} e^{\frac{V_{Bias} - (V_{th} - \eta V_{DIBL})}{nV_T}}$

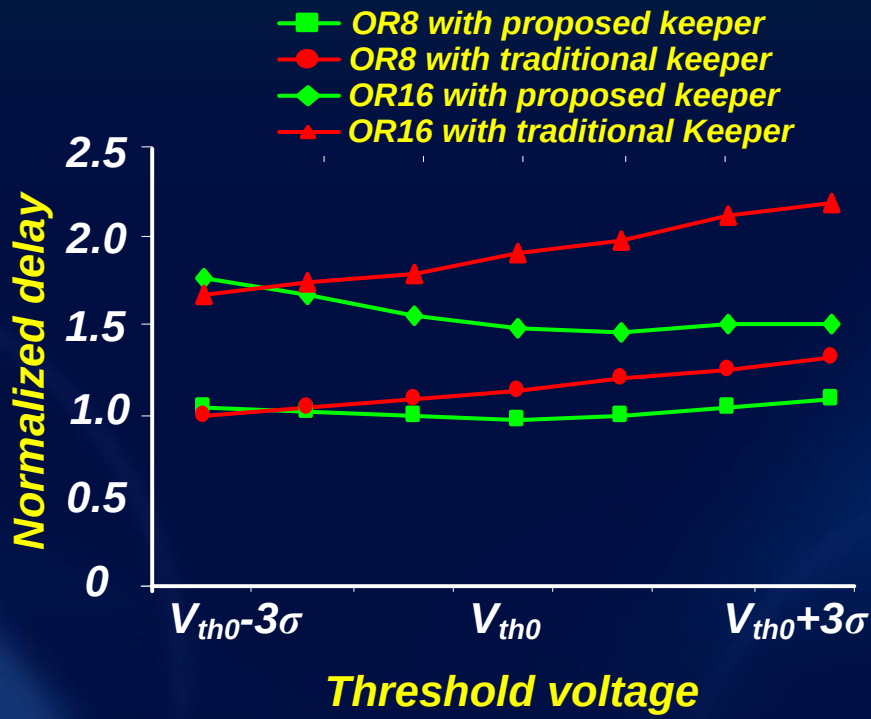
(b) I_{REF} **and** V_{Bias} **are function of** nV_T.

(c) $V_{th} - \eta V_{DIBL} = cons.$

- I_{REF} and V_{Bias} are designed to be independent of V_{th} and it's variations.
- M_2 is biased to operate in sub-threshold region.
- Small variation in V_{th} of M_2 causes η time wider fluctuation on V_{DIBL}. (η is DIBL constant).

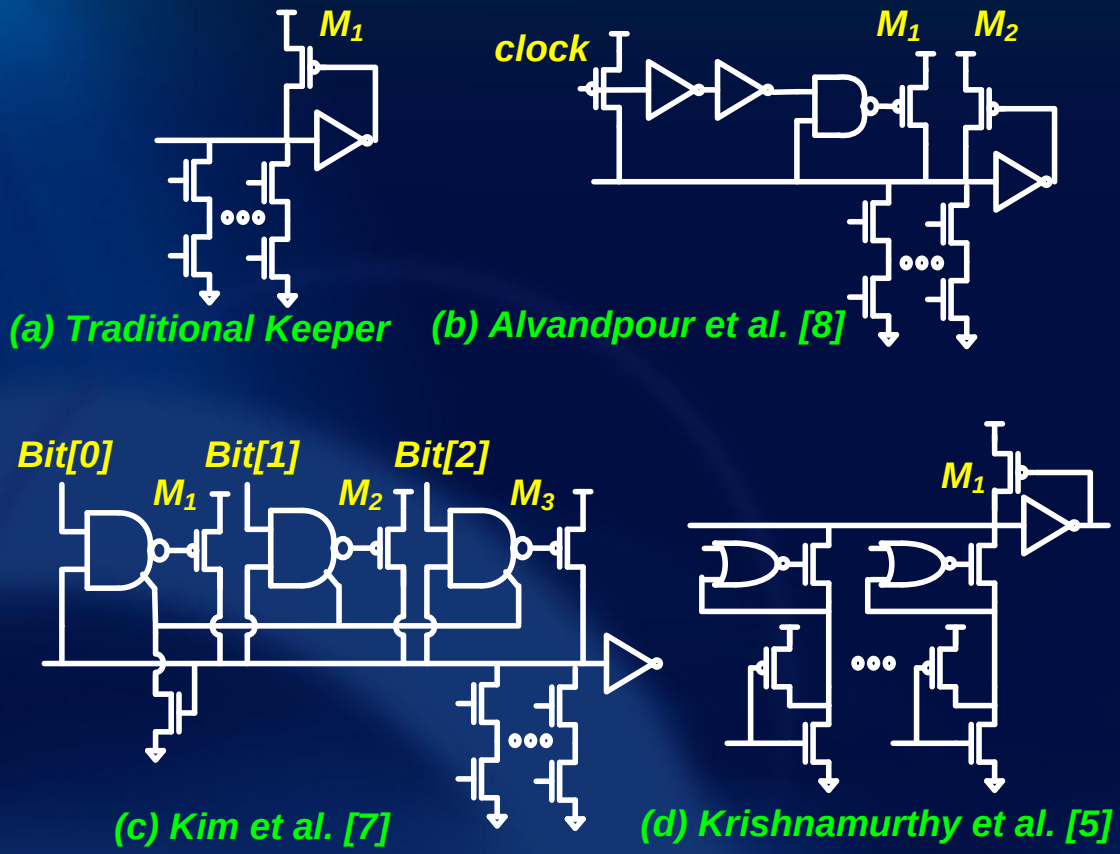
Implementation and Results





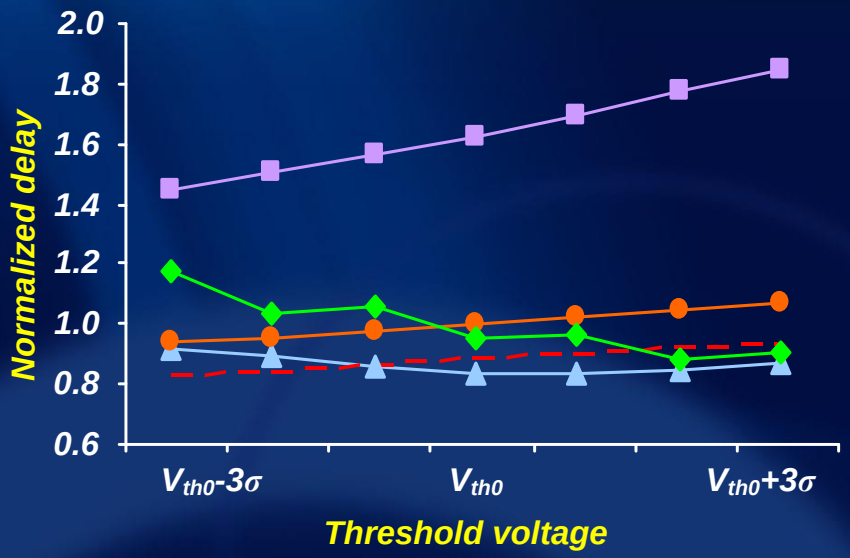
- Normalized current supplied by traditional and proposed keeper vs minimum required current. (left)
- Normalized delay of 8- and 16-input OR gates with traditional and proposed keeper. (right)

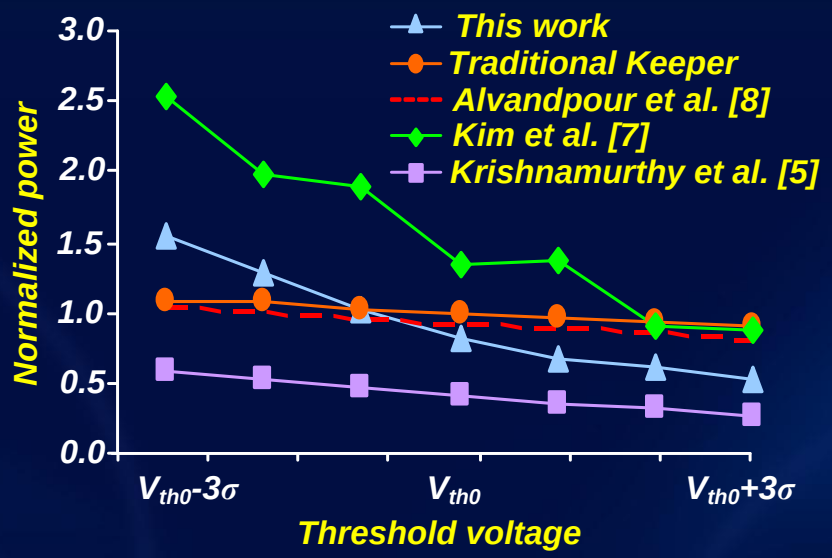
Proposed Keeper



- Proposed keeper has been compared to previous work.
- Mean delay value, power consumption and standard deviation of delay are used as metrics.

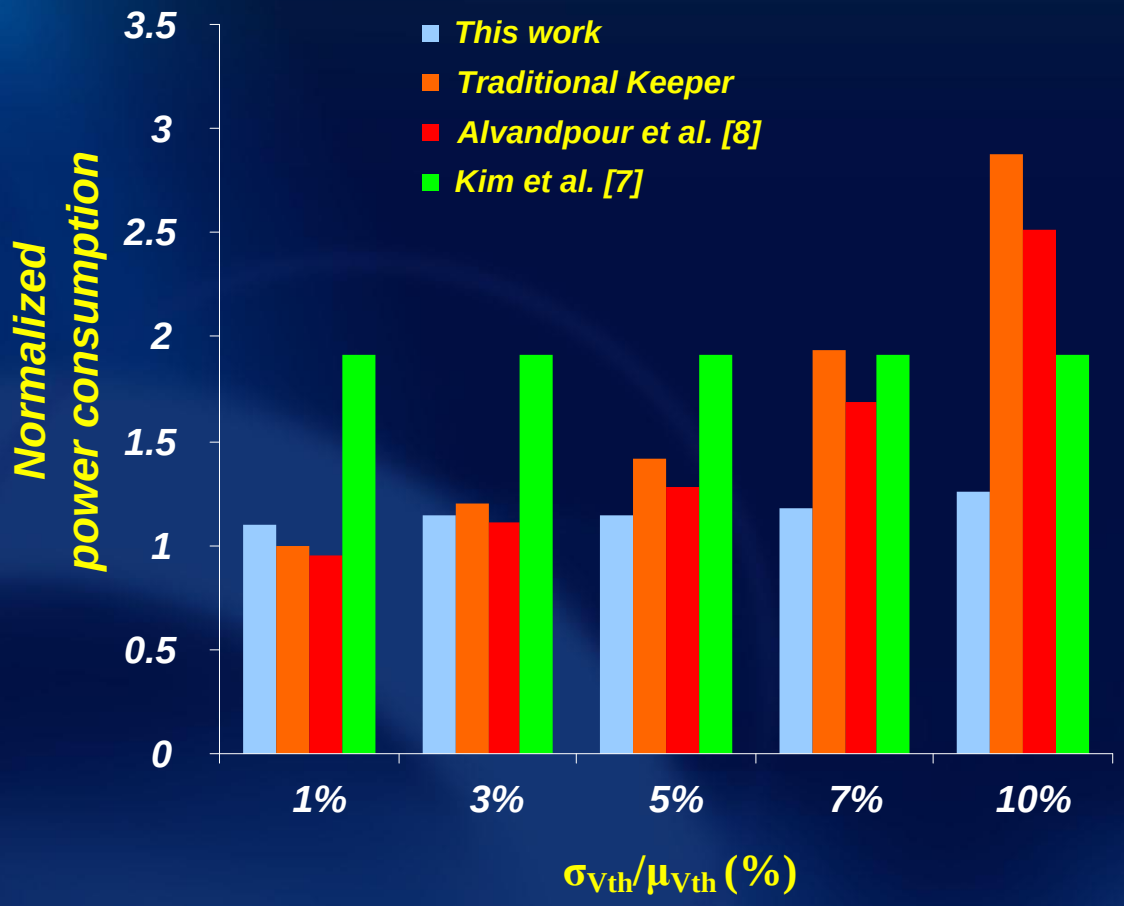
Implementation and Results





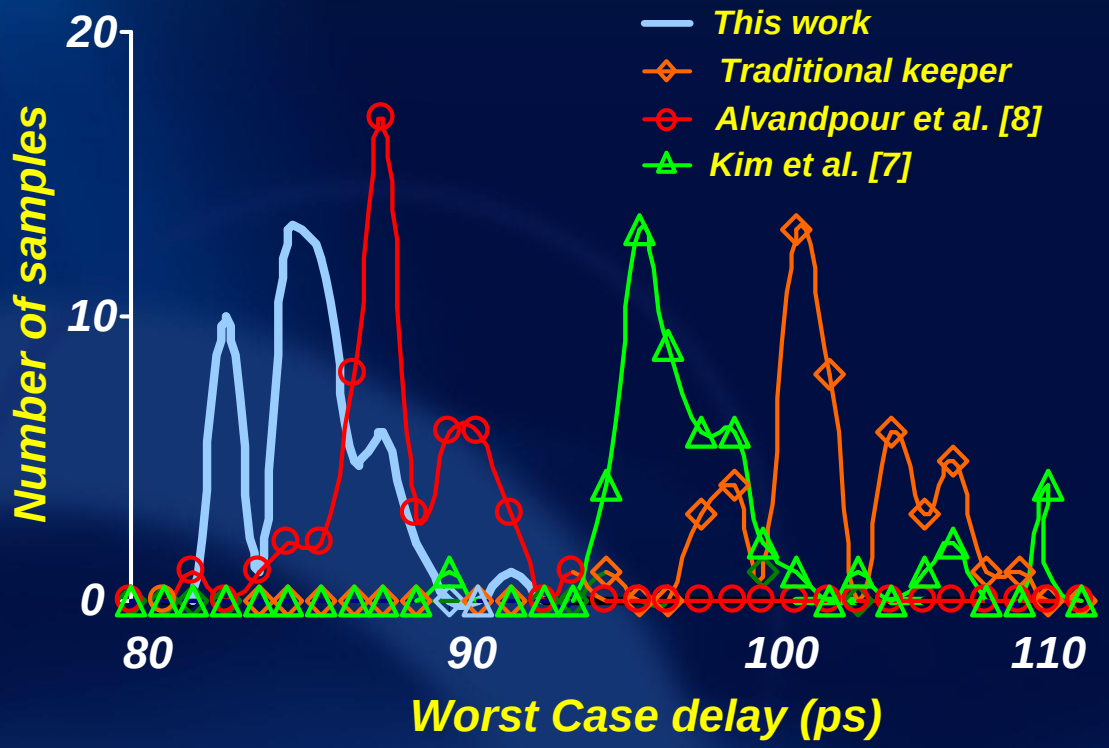
- **Comparison between normalized mean delay (left) and power consumption (right) of OR gates realized by different keepers.**
- **Proposed keeper shows low delay and power consumption.**

Implementation and Results



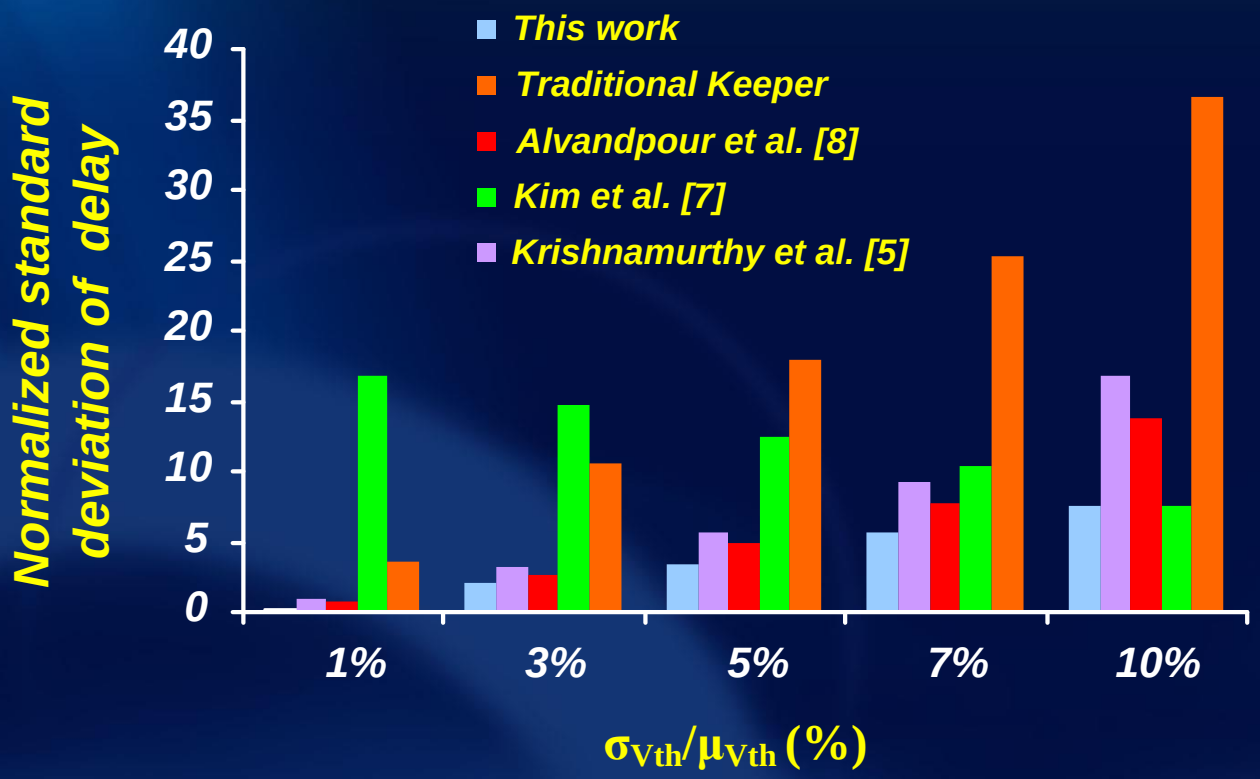
- **Normalized power consumption for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).**

Implementation and Results



- Delay distribution of dynamic OR gates with different keeper circuits obtained for 100 samples.
- Distribution corresponded to proposed keeper shows lower mean and narrower spread.

Implementation and Results



- Normalized STD of delay for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).
- Proposed keeper shows superior behavior in terms of robustness to increasing level of variation.

Conclusions

- **A novel approach for designing low-power variation-aware keeper circuits of wide fan-in dynamic gates has been presented.**
- **Through a graphical representation, it was shown that conventional keeper circuits generate unnecessary excess contention that can be avoided with proper design of keeper.**
- **HSPICE simulation results show that the proposed architecture offers smallest delay deviation for entire *Vth* range considered in this study, compared to all existing works in the literature.**
- **The proposed keeper architecture could be very effective in increasing the robustness of dynamic gates to process variation.**