CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With $\leq$ 50-mV/decade Subthreshold Swing

Ramanathan Gandhi, Zhixian Chen, Navab Singh, *Senior Member, IEEE*, Kaustav Banerjee, *Senior Member, IEEE*, and Sungjoo Lee

***Abstract*—We present a vertical-silicon-nanowire-based p-type tunneling field-effect transistor (TFET) using CMOS-compatible process flow. Following our recently reported n-TFET [11], a low-temperature dopant segregation technique was employed on the source side to achieve steep dopant gradient, leading to excellent tunneling performance. The fabricated p-TFET devices demonstrate a subthreshold swing (SS) of 30 mV/decade averaged over a decade of drain current and an $I_{\rm on}/I_{\rm off}$ ratio of $> 10^5$. Moreover, an SS of 50 mV/decade is maintained for three orders of drain current. This demonstration completes the complementary pair of TFETs to implement CMOS-like circuits.**

***Index Terms*—CMOS technology, gate all around (GAA), steep subthreshold slope, subthreshold swing (SS), top–down, tunneling field-effect transistor (TFET), vertical silicon nanowire (SiNW).**

I. Introduction

CMOS device scaling, which has continued for more than the last four decades, is facing severe challenges as a result of excessive increase in power consumption caused by increasing OFF-state leakage and nonscalability of the operating voltage ($V_{\rm dd}$). $V_{\rm dd}$ scaling requires simultaneous scaling of threshold voltage ($V_{\rm th}$) for maintaining a certain ON-to-OFF ratio of the device currents, which however leads to a substantial increase in the subthreshold leakage (OFF state) current, owing to the nonscalability of the subthreshold swing (SS) of MOSFETs. The SS in MOSFETs is governed by thermal diffusion of carriers over a potential barrier and has a theoretical lower limit of 60 mV/decade at room temperature [1]. Tunneling field-effect transistors (TFETs) employ a fundamentally different injection mechanism in the form of band-to-band tunneling [2] to achieve SS that is lower than 60 mV/decade [3]–[9].

Although there are a few TFETs reporting lower than 50 mV/decade using carbon nanotubes [3], heterostructures [4], or complex TFET structures [5], achieving $SS <$ 50 mV/decade has been challenging in most of the fabricated TFETs [7], [9], [10]. Hence, there is significant interest in designing and fabricating Si TFETs with low SS. Recently, we have reported a fully CMOS-compatible novel homojunction n-TFET with SS as low as 30 mV/decade [11]. The device utilized a low-temperature dopant segregation technique on the source side with vertical gate-all-around (GAA) architecture having a cylindrical nanowire as the channel/body. In this letter, we focus on p-TFETs to complete the complementary pair using the same process technology and device architecture so that they can be implemented into CMOS-like circuits. Following our n-TFET footsteps, our p-TFET also demonstrates an SS of 30 mV/decade over a decade of drain current and an $I_{\rm on}/I_{\rm off}$ ratio of $> 10^5$. To the best of our knowledge, this is the lowest ever reported SS for any experimental p-TFET device. Moreover, our p-TFETs exhibit $SS \leq$ 50 mV/decade for three orders of drain current. It is worth mentioning that, besides a much smaller footprint and achieving low SS, the vertical nanowire devices are ideal platform for TFET due to self-decoupling of source and drain implants.

II. Device Fabrication

The device fabrication followed exactly the same steps as reported for n-TFET [11] except interchanging the type of implants in source/drain and gate and reducing the drain-side underlap to optimize the drive current [Fig. 1(a)]. In brief, on p-type (Boron $\sim 10^{15}$ cm^{-3}) 8-in bulk Si wafers, 400-nm-tall vertical Si nanowires (SiNWs) with diameters from 20 to 200 nm and Si_3N_4 cap on top were obtained using deep ultraviolet lithography, reactive ion etching, and sacrificial oxidation process, respectively. BF_2 implantation (10^{15} cm^{-2}/10 keV/0° tilt) and activation (1000 °C/10 s) were then performed to define the drain region. Two-hundred-nm-thick high-density plasma (HDP) oxide, which (being nonconformal) is much thinner on the sidewall than the horizontal surface, was deposited and etched back partially using diluted hydrofluoric acid (DHF) to obtain 35-nm isolation oxide. Thereafter, a gate oxide of 4.5 nm was thermally grown,

Manuscript received July 15, 2011; accepted August 6, 2011. Date of publication September 25, 2011; date of current version October 26, 2011. The review of this letter was arranged by Editor J. Cai.

R. Gandhi is with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685, and also with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576 (e-mail: g0900317@nus.edu.sg).

Z. Chen and N. Singh are with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685 (e-mail: chenzx@ime.a-star.edu.sg; navab@ime.a-star.edu.sg).

K. Banerjee is with the Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: kaustav@ece.ucsb.edu).

S. Lee is with the SKKU Advanced Institute of Nanotechnology, Sungkyunkwan University, Suwon 440-746, Korea (e-mail: leesj@skku.edu).

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Digital Object Identifier 10.1109/LED.2011.2165331

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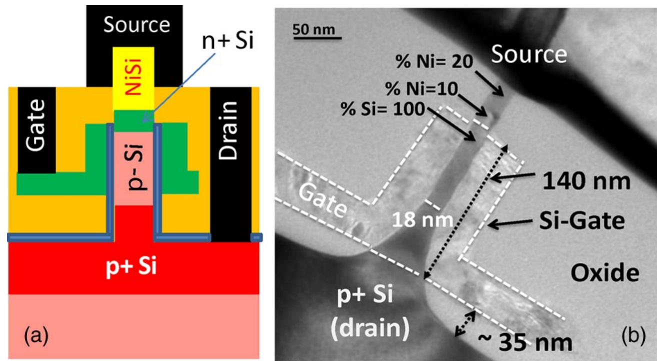

Fig. 1. (a) Device schematic and (b) TEM image of the fabricated device with a nanowire diameter of ∼18 nm and a gate length of ∼140 nm.

followed by 50-nm amorphous-Si deposition using low-pressure chemical vapor deposition.

Gate was implanted vertically by using phosphorus (10^{15} cm^{-2}/10 keV) and activated at 1000 °C for 5 s. HDP oxide deposition and etch back were repeated, and the exposed amorphous Si was isotropically etched, thus defining the gate length. A gate pad serving as extension for a gate contact was lithographically patterned and etched. Arsenic (10^{15} cm^{-2}/5 keV) was then implanted from four directions—90° apart at a tilt angle of 60° to form the n^+ source region. As the drain terminal was embedded inside, no lithography step to define the source implant (to protect the drain) was needed. Isolation HDP oxide was again deposited, and DHF back etch was once again used to create a thin spacer between the gate edge and source of the nanowire. It was to prevent the gate from being shorted to source in the following silicidation process.

Thereafter, Ni (15 nm) was deposited by sputtering and followed by a two-step rapid thermal annealing (RTA) at 220 °C/30 s and 440 °C/30 s in N_2 ambient. Unreacted Ni was selectively removed after the first RTA in $H_2SO_4 : H_2O_2 : H_2O$ solution, leaving NiSi around the source of nanowire. The purpose of this step was to segregate Arsenic dopants at the silicide–silicon interface, which is also the source-to-channel junction. Finally, pre-metal dielectric was deposited and followed by Al metallization and sintering process.

A transmission electron microscopy (TEM) image of the fabricated device, along with the device schematic, is shown in Fig. 1(b). A nanowire of diameter 18 nm with silicided top and surrounding poly-Si ($L_G = 140$ nm) can be clearly seen. Through energy dispersive X-ray analysis, we found that, in the silicided tips, the Ni concentration was rather low and it reduced further toward the source–channel junction, indicating room for further improvement.

III. Results and Discussion

An HP4156A parameter analyzer was used to characterize the TFETs. Shown in Fig. 2 are the transfer and output characteristics of the device having a nanowire diameter of ∼18 nm and a gate length of ∼140 nm (the device image in Fig. 1). Average SS values of 30 and 50 mV/decade are achieved for a decade (10^{-14}–10^{-13} A) of drain current and three orders of drain current (10^{-14}–10^{-11} A), respectively. We measured the gate leakage to ensure that steep subthreshold slope is not an artifact of leakage effects, and it was indeed found to remain at noise level. In addition, temperature-dependent measurements were conducted, and the results were found to be consistent with the temperature dependence of ON current shown and discussed in our earlier n-TFET work [11].

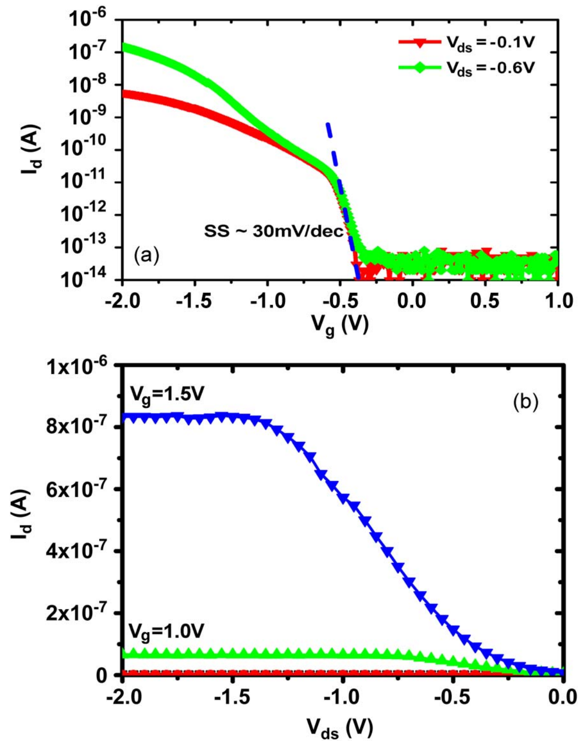

Fig. 2. (a) I_d–V_g characteristic of a vertical-SiNW pTFET device with low SS values of 30 and 50 mV/decade over 10^{-14}–10^{-13} A and 10^{-14}–10^{-11} A of drain current, respectively, and (b) corresponding I_d–V_{ds} characteristics.

Suppression of ambipolar conduction is achieved because of natural asymmetry of the vertical nanowire platform, which facilitated independent tuning of source and drain doping. Indeed, drain was implanted first and subjected to high thermal budget. On the other hand, source was implanted later at the very final stage of the fabrication, and a low-temperature dopant-segregated silicidation method was employed to pile up dopants toward the source–channel junction.

Fig. 3 emphasizes the observed increase in SS with increasing drain current, which is a typical phenomenon in TFETs, differentiating their I–V characteristics from those of MOSFETs [2]. Variations in SS as a function of nanowire diameter are shown in Fig. 4. It can be observed that, as the channel diameter increases, SS increases. When the channel gets wider, the gate electrostatic control on the channel region becomes weaker, and the device behaves more like a planar device. Moreover, for larger diameter wires, the encroachment of NiSi into the wire is weak [12], thereby keeping the silicide–silicon interface far from the source–channel junction. In such case, the dopant gradient at the source–channel junction is expected to be less steep, hence degrading SS. Furthermore, the higher variability in SS with increasing diameter is yet to be understood.

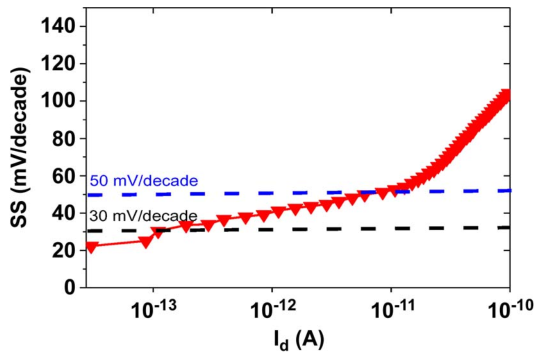

Fig. 3. I_d-versus-SS plot showing the typical TFET behavior and sub-50-mV/decade SS for three decades of drain current (10^{-14}–10^{-11} A).

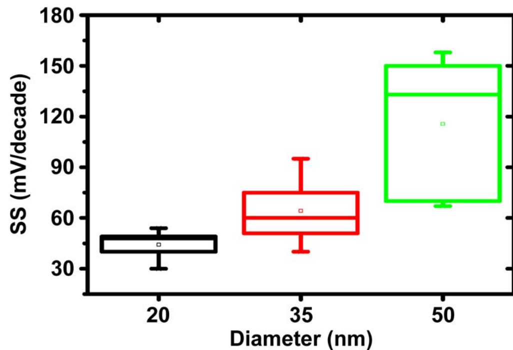

Fig. 4. Dependence of SS on nanowire diameter. The SS is taken at $V_{\rm ds} = -0.1$ V, and the current level is 10^{-14} to 10^{-13} A. Five devices were measured for each diameter.

It is important to note that the ON current achieved in this work ($\sim$1.2 μA/μm at $V_{\rm DD} = -1$ V; normalized to the width of the wire) is much larger than our previously reported ON current for n-TFET device ($\sim$0.02 μA/μm) [11]. This is because of the difference in the gate–drain underlap; the p-TFET has an underlap of $\sim$35 nm (as shown in Fig. 1) while the n-TFET has a large underlap of $\sim$100 nm. Large underlap on the drain side seems to be one of the reasons suppressing the ON current of n-TFET (due to nonuniform potential along the channel region under a gate bias). This implies that optimum gate–drain underlap is required to suppress ambipolar conduction, as well as to maximize ON current. The difference in the diffusivity of the source dopants (As for p-TFET and BF_2 for n-TFET) could be another reason for the difference in the ON current between these two devices. Dopants redistribute after silicide formation due to the generation of point defects [13], and since BF_2 is a fast diffusive species compared to As, the source–channel junction could be more graded in n-TFET devices, thereby resulting in smaller tunneling current.

IV. Conclusion

We have presented a vertical-SiNW-based p-type TFET device with a record low SS of 30 mV/decade observed over a decade of drain current and an $I_{\rm on}/I_{\rm off}$ ratio of $> 10^5$. In addition, a sub-50-mV/decade value was observed for three orders of drain current. This work substantiates TFET in vertical GAA nanowire architecture as a potential candidate for future energy-efficient electronics. Moreover, by using other known designs like heterostructure-based TFETs with smaller bandgap material at the tunneling interface [6] as well as high-k gate dielectrics [6], [8], one can achieve further enhancement in ON current.

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