Compact AC Modeling and Performance Analysis of Through-Silicon Vias in 3-D ICs

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***Abstract*—This paper introduces the first comprehensive and accurate compact resistance–inductance–capacitance–conductance ($RLCG$) model for through-silicon vias (TSVs) in 3-D ICs valid from low- to high-frequency regimes, with consideration of the MOS effect in silicon, the alternating-current (ac) conduction in silicon, the skin effect in TSV metal, and the eddy currents in the silicon substrate. The model is verified against electrostatic measurements as well as a commercial full-wave electromagnetic simulation tool and subsequently employed for various performance (delay) analyses. The compact model is also applicable to TSVs made of carbon nanotube (CNT) bundles, once a slight modification (making the effective conductivity complex) is made. Various geometries (as per the International Technology Roadmap for Semiconductors) and prospective materials (Cu, W, and single-walled/multiwalled CNTs) are evaluated, and a comparative performance analysis is presented. It is shown that CNT-bundle-based TSVs can offer smaller or comparable high-frequency resistance than those of other materials due to the reduced skin effect in CNT bundle structures. On the other hand, the performance (delay) analysis indicates that the performance differences among different TSV materials are rather small. However, it is shown that CNTs provide an improved heat dissipation path due to their much higher thermal conductivity. In addition, the improved mechanical robustness and thermal stability of CNTs also favor their selection as TSV materials in emerging 3-D ICs.**

***Index Terms*—Carbon nanotube (CNT), complex conductivity, interconnect, resistance–inductance–capacitance–conductance ($RLCG$) model, thermal analysis, through-silicon via (TSV), 3-D IC.**

I. Introduction

THREE-DIMENSIONAL integration to create multilayer chips (3-D ICs) offers an exciting alternative to traditional scaling, wherein continuous increase in functionality, performance, and integration density can be sustained indefinitely by stacking semiconductor layers on top of each other in an "integrated" manner [1]. Three-dimensional ICs also offer the most promising platform to implement "More-than-Moore" technologies, bringing heterogeneous materials [Silicon, III–V semiconductors, carbon nanotube (CNT)/graphene, etc.] and technologies (memory, logic, radio frequency, mixed signal, microelectromechanical systems, optoelectronics, etc.) on a single chip [1], [2]. High-aspect-ratio vertical interconnects, called through-silicon vias (TSVs), providing connectivity between active layers, constitute a key technology for 3-D ICs (Fig. 1) [3]. While fabrication technologies of TSVs have progressed [4]–[8], there is a need to accurately and efficiently evaluate their admittance/impedance in a broadband frequency regime for performance analysis and subsequent design optimization. There are several approaches to model the admittance/impedance of TSVs. The capacitance and resistance of TSVs are modeled in [9], but the silicon substrate is treated as a good conductor, which is not accurate for high-frequency analysis, and the inductance is ignored. Although the modeling of inductance of the TSVs is included in [10], the silicon substrate is simply treated as a dielectric, implying that the ac conduction and eddy currents in silicon are not taken into account.

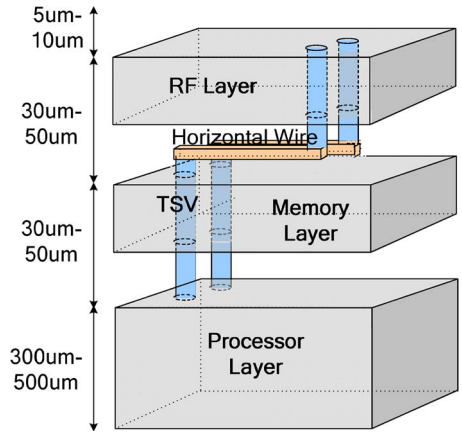

Fig. 1. Schematic of a 3-D IC with high-aspect-ratio TSVs (the diameters of the TSVs are typically smaller than 10 μm).

The approach employing full-wave numerical simulation [11] is accurate but slow and memory intensive and, as such, not suitable for large-scale analysis and design optimization. In addition, [9]–[11] have not taken into account the depletion region surrounding the TSV dielectrics (MOS effect), while this effect has a key impact on the capacitance model, as pointed out in [3], [8], and [12]–[14]. However, the models in [12]–[14] also have their own limitations. In [12] and [13], the depletion region model simply ignores the interface charge. This assumption is only valid if the isolation dielectric is thermally grown SiO_2

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at a high temperature as in [15], where the interface charge density is low. The assumption is not valid in state-of-the-art TSV technologies, where the via-hole etching and isolation SiO_2 is usually formed after the front-end-of-line processes [6], [8], because the Si-SiO_2 interface charge, which is induced by plasma damage during via-hole etching or dielectric deposition [16], cannot easily be removed due to the lack of subsequent high-temperature processes. Furthermore, the equations in [12] are mainly empirical, which lack physical insight and are not valid in general conditions.[1] In [14], the MOS effect including the impact of the interface charge is discussed from experimental, numerical simulation, and analytical analyses, but there are errors in their analytical equations (which will be explained in Section II). Furthermore, the performance analysis (inverter chain delay) in [14] is based on a distributed RC model of TSVs, by claiming that the inductance can be ignored since clock frequencies are below 3 GHz. However, this "cause-and-effect" logic is not valid in state-of-the-art technologies, because the significant frequency (reflecting the highest frequency of concern in signal propagation) is much higher than the clock frequency [17], [18].

Recently, CNT interconnects and passive devices have been investigated. Their low electrical resistivity [19], [20], reduced skin effect [21], [22], high thermal conductivity [23], and current carry capacity [19] merit additional attention. In general, it is easier to grow CNTs in the vertical direction, and CNT-based TSVs have been fabricated [24]. It has been shown in [25] and [3] that tall CNT-bundle-based vias, with height greater than the electrical and thermal mean free path (MFP), may provide significant advantages in terms of both electrical and thermal characteristics. Therefore, both electrical and thermal analyses of CNT-based TSVs are desirable to evaluate their relative performance *vis-à-vis* Cu and W based TSVs.

In this paper, accurate electrostatic and high-frequency compact models for TSVs are developed that are applicable for both traditional metals (such as Cu and W) and CNTs. By treating CNT bundles as an equivalent material with "complex effective conductivity," the resistance and inductance are calculated and compared with those of Cu and W. Their $RLCG$ parameters under scaling and the performance of different TSV materials at the 22-nm technology node are subsequently analyzed. A comparative thermal analysis among Cu, W, and CNT bundle based TSVs is also presented.

II. Electrostatics of TSVs (MOS Effect)[2]

The top cross-sectional view of a typical TSV is shown in Fig. 2. The TSV is surrounded by a dielectric (usually SiO_2) for dc isolation. For Cu TSVs, an ultrathin barrier metal

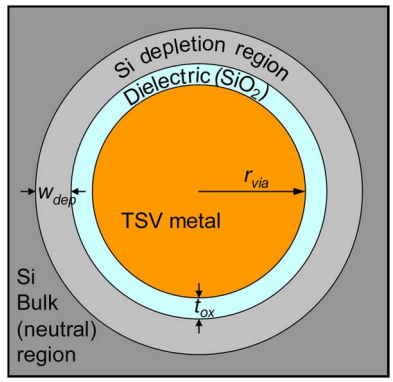

Fig. 2. Top cross-sectional view of a TSV surrounded by the dielectric (SiO_2), the Si depletion region, and the bulk Si.

(usually Ta) is required between Cu and the dielectric to avoid diffusion of Cu atoms. The isolation dielectric may or may not be surrounded by a depletion region, depending on the voltage bias condition, interface charge density, material properties of the surrounding Si (n/p-type, electrical conductivity, etc.), and geometrical parameters of the TSV [3]. If the TSV height is much greater than its diameter, a 2-D approximation of electrostatics can be assumed, i.e., the Poisson equation surrounding a TSV (assuming a p-type Si substrate) can be expressed as

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\psi}{dr}\right) = \begin{cases} qN_a/\varepsilon_{\rm Si}, & r_{\rm via}+t_{\rm ox} < r < r_{\rm via}+t_{\rm ox}+w_{\rm dep} \\ 0, & r_{\rm via} < r < r_{\rm via}+t_{\rm ox} \end{cases} \quad (1)$$

where the geometrical parameters $r_{\rm via}$, $t_{\rm ox}$, and $w_{\rm dep}$ are the radius of the via, the thickness of the isolation dielectric, and the Si depletion width (see Fig. 2); $\psi(r)$ is the electrical potential as a function of the radius (r); N_a is the p-type bulk doping concentration; q is the elementary charge; and $\varepsilon_{\rm Si}$ is the permittivity of Si. The boundary conditions can be expressed as

$$\begin{cases} \psi(r_{\rm via}+t_{\rm ox}+w_{\rm dep}) = 0 \\ \psi(r_{\rm via}) = V+\phi_{\rm ms} \\ \left.\frac{d\psi}{dr}\right|_{r=r_{\rm via}+t_{\rm ox}+w_{\rm dep}} = 0 \\ \varepsilon_{\rm Si}\left.\frac{d\psi}{dr}\right|_{r=r_{\rm via}+t_{\rm ox}+\Delta r} + Q_i = \varepsilon_{\rm ox}\left.\frac{d\psi}{dr}\right|_{r=r_{\rm via}+t_{\rm ox}-\Delta r} \end{cases} \quad (2)$$

where V is the bias voltage of the TSV; $\varepsilon_{\rm ox}$ is the permittivity of the dielectric; Q_i is the interface charge density; and $\phi_{\rm ms}$ is the work function difference between the TSV metal or (in the case of a Cu TSV) TSV barrier metal (e.g., Ta with a work function of 4.25 eV) and doped silicon. Here, $r = r_{\rm via}+t_{\rm ox}+w_{\rm dep}$ indicates the position at the boundary of the Si bulk and depletion region; Δr is an infinitesimal value; and $r = r_{\rm via}+t_{\rm ox}+\Delta r$ or $r = r_{\rm via}+t_{\rm ox}-\Delta r$ indicates the Si or SiO_2 side at the Si-SiO_2 interface, respectively. By solving the Poisson equation (1) and boundary conditions (2), the implicit expression for solving $w_{\rm dep}$ can be derived [3]. In particular, in depletion/weak inversion condition, where negligible free charges (carriers) exist on the Si-SiO_2 interface, the total charge including the depletion

[1]For example, the α term in [12, (2), (3), (5) and (6)] is claimed to account for the current loss in the substrate, but the substrate conductivity, permittivity, and frequency are not explicitly shown in [12, (5) and (6)], implying that these two equations can only be valid for a specific condition.

[2]The modeling of the MOS effect is simultaneously but independently developed in [3] and [14], based on the same physical concepts. However, there are errors in the final equations in [14]. First, in [14, (A2)], the term $2\ln(N_a/n_i)$ should be $(2k_bT/q)\ln(N_a/n_i)$, as shown in (4) of this paper. Second, in [14, (A5)], the term $2\ln(N_a/n_i)$ should be replaced with $\psi(R_{\rm ox})$ in [14], which is equivalently written as $\psi(r_{\rm via}+t_{\rm ox})$ in (3) of this paper.

and interface charge can be written as

$$\pi\left[(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2-(r_{\rm via}+t_{\rm ox})^2\right]\cdot qN_a - 2\pi(r_{\rm via}+t_{\rm ox})Q_i = [V-\phi_{\rm ms}-\psi(r_{\rm via}+t_{\rm ox})] \cdot 2\pi\varepsilon_{\rm ox}/\ln\left(1+\frac{t_{\rm ox}}{r_{\rm via}}\right) \quad (3a)$$

while the electrical potential at the Si-SiO_2 interface can be expressed as

$$\psi(r_{\rm via}+t_{\rm ox}) = \frac{qN_a}{2\varepsilon_{\rm Si}}\cdot\left[(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2\ln\left(1+\frac{w_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right) -\frac{1}{2}w_{\rm dep}^2-w_{\rm dep}(r_{\rm via}+t_{\rm ox})\right]. \quad (3b)$$

One can also interpret (3) through its physical implications: (3a) essentially represents Gauss's law, while (3b) is the integration of the Poisson equation (1) in the depletion region. There are two unknowns in the two equations of (3), i.e., $w_{\rm dep}$ and the potential drop in the depletion region $\psi(r_{\rm via}+t_{\rm ox})$, which can be solved self-consistently. For the maximum depletion region condition, the electrical potential drop across the depletion region can be written as

$$\frac{2k_BT}{q}\cdot\ln\left(\frac{N_a}{n_i}\right)=\frac{qN_a}{2\varepsilon_{\rm Si}}\left[-\frac{1}{2}w_{\rm dep}^2-w_{\rm dep}\,(r_{\rm via}+t_{\rm ox}) +(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2\ln\left(1+\frac{w_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right)\right] \quad (4)$$

where n_i is the intrinsic carrier concentration of Si. Here, the physical meaning of (4) is similar to that in (3b), but $\psi(r_{\rm via}+t_{\rm ox})$ is almost fixed at $2\phi_F=(2k_BT/q)\cdot\ln(N_a/n_i)$. Consequently, the middle-frequency capacitance[3] per unit height between the TSV and the substrate $(C_{\rm MF})$ can be obtained [3] as follows:

$$C_{\rm MF}=\left(\frac{1}{C_{\rm ox}}+\frac{1}{C_{\rm dep}}\right)^{-1} =\left[\frac{1}{2\pi\varepsilon_{\rm ox}}\cdot\ln\left(1+\frac{t_{\rm ox}}{r_{\rm via}}\right)+\frac{1}{2\pi\varepsilon_{\rm Si}}\cdot\ln\left(1+\frac{w_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right)\right]^{-1}. \quad (5)$$

[3]The middle-frequency capacitance is equivalent to the "high-frequency capacitance" of MOS capacitors in semiconductor device physics: at such frequencies (~1 MHz), the generation/recombination of inversion carriers or the charging/discharging of interface states cannot follow the fast signals. However, the term "high frequency" has different meanings in this paper: at such frequencies (> 1 GHz), the ac conduction of bulk Si takes effect on the capacitance and conductance of the TSVs. To avoid conflict, we use the term "middle frequency" to represent the previous case. In addition, this paper assumes a small signal capacitance at all frequencies (not the deep depletion mode capacitance), because the power supply (or realistic bias) voltage ($V_{\rm DD}$, around 1 V) is usually less than the difference between the threshold voltage and the flat-band voltage.

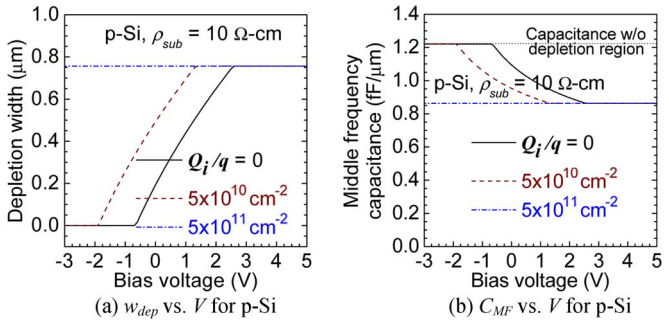

Fig. 3. Electrostatic result of a TSV surrounded by SiO_2 and p-type Si: (a) depletion width and (b) middle-frequency (~MHz) capacitance as a function of the bias voltage and Si/SiO_2 interface charge density (Q_i). [$r_{\rm via}=2.5$ μm; $t_{\rm ox}=0.5$ μm; the barrier metal is Ta (a work function of 4.25 eV); the Si bulk resistivity is 10 Ω-cm ($N_a=1.25\times10^{15}$ cm^{-3}, which corresponds to a work function of 4.89 eV)].

Similarly, the electrostatics of the TSV surrounded by an n-type Si substrate can also be obtained. In particular, (3) and (4) can be replaced by the following: in depletion condition, we have (6), shown at the bottom of the page, whereas the condition with maximum depletion region is

$$\frac{2k_BT}{q}\cdot\ln\left(\frac{N_d}{n_i}\right)=\frac{qN_d}{2\varepsilon_{\rm Si}}\left[-\frac{1}{2}w_{\rm dep}^2-w_{\rm dep}(r_{\rm via}+t_{\rm ox}) +(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2\ln\left(1+\frac{w_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right)\right]. \quad (7)$$

Using (3) and (4) or (6) and (7), we can obtain the $w_{\rm dep}$ of a TSV with typical geometrical parameters ($r_{\rm via}=2.5$ μm, $t_{\rm ox}=0.5$ μm) and surrounded by either p-type or n-type Si (bulk resistivity is 10 Ω-cm). The results of $w_{\rm dep}$ as a function of the bias voltage (V) are shown in Figs. 3(a) and 4(a), while the middle-frequency C–V curves are shown in Figs. 3(b) and 4(b). It can be observed that a significant error in capacitance will be induced if the depletion region is not considered. Notice that the capacitance is not only dependent on geometrical parameters but also on the Si/SiO_2 interface charge, semiconductor type, and bias voltage.

Our MOS effect model is verified against the experimental and numerical simulation results in [14, Fig. 3(b)]. With the parameters provided in [14] ($r_{\rm via}+t_{\rm ox}=2.5$ μm; $t_{\rm ox}=118.2$ nm; $N_a=2\times10^{15}$ cm^{-3}; $\varepsilon_{\rm ox}=3.9\varepsilon_0$; and TSV height $=20$ μm), the calculated capacitance in accumulation condition using our model is 89.6 fF, as compared to 89 fF from the numerical simulation and 84 fF from measurement result in [14]; the calculated capacitance for the maximum depletion region condition, using our model is 36.1 fF, as compared to 37 fF from the numerical simulation and 34 fF from measurement result in [14].

As explained in the introduction, the Si-SiO_2 interface charge, which is induced by plasma damage during via-hole

$$\begin{cases}\pi\left[(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2-(r_{\rm via}+t_{\rm ox})^2\right]\cdot qN_d+2\pi(r_{\rm via}+t_{\rm ox})Q_i=-[V-\phi_{\rm ms}-\psi(r_{\rm via}+t_{\rm ox})]\cdot2\pi\varepsilon_{\rm ox}/\ln\left(1+\frac{t_{\rm ox}}{r_{\rm via}}\right)\\ \psi(r_{\rm via}+t_{\rm ox})=-\frac{qN_d}{2\varepsilon_{\rm Si}}\cdot\left[(r_{\rm via}+t_{\rm ox}+w_{\rm dep})^2\ln\left(1+\frac{w_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right)-\frac{1}{2}w_{\rm dep}^2-w_{\rm dep}(r_{\rm via}+t_{\rm ox})\right]\end{cases} \quad (6)$$

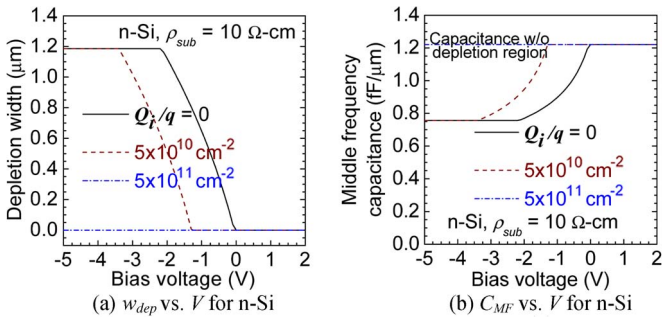

Fig. 4. Electrostatic result of a TSV surrounded by SiO_2 and n-type Si: (a) depletion width and (b) middle-frequency (∼MHz) capacitance as a function of the bias voltage and Si/SiO_2 interface charge density (Q_i) [resistivity is 10 Ω-cm ($N_d = 4.46 \times 10^{14}$ cm^{-3}), and all other parameters are the same as in Fig. 3]. Note that, as Q_i becomes high enough, the flatband voltage becomes even more negative. Hence, in the bias voltage range of concern (-5 V $< V_{\rm bias} < 2$ V), the MOS structure is in the accumulation mode, resulting in $w_{\rm dep} = 0$.

etching or dielectric deposition [16], cannot easily be removed. In the following analysis, a p-type Si substrate with a resistivity of 10 Ω-cm and a large interface charge density ($\sim 5 \times 10^{11}$ cm^{-2}) is assumed, which implies a saturated depletion width and middle-frequency capacitance, independent of the (low) bias voltage (see Fig. 3), due to Fermi level pinning at the Si-SiO_2 interface. Note that this assumption leads to full agreement with the experimental C–V curve in [8] and [14], where the "threshold voltage" is very negative.

III. Compact $RLCG$ Model for TSVs

Signals on interconnects propagate over a wide range of frequencies with the highest frequency of concern or significant frequency (f_B) determined by the signal rise/fall time (t_r), being much higher than the clock frequency in a digital system ($f_B \propto t_r^{-1}$) [17]. In 45-nm technology, f_B can be as high as 62 GHz [18]. Hence, a simple treatment of TSV interconnects as RC elements is insufficient at high frequencies. In this paper, using an equivalent circuit [Fig. 5(a)], the ac conduction in the silicon substrate (from $\mathrm{Re}(Y_2)$), the skin effect in the TSV metal (from $Z_{\rm metal}$), and eddy currents (from $R_{\rm sub}$) in silicon are included for high-frequency analysis (the terminologies will be explained later).[4]

The equivalent circuit in Fig. 5(a) can further be reduced to a simplified transmission line model [Fig. 5(b)], containing two components: parallel admittance per unit TSV height ($Y = G + jB$, where G and B are the equivalent conductance and susceptance, respectively) and serial impedance per unit TSV height ($Z = R + jX$, where R and X are the equivalent resistance and reactance, respectively). Furthermore, the open-circuit total admittance $Y_{\rm open}$ and the short-circuit total impedance $Z_{\rm short}$ are defined in Fig. 5(b). Since $\sqrt{|ZY|}H \ll 1$ at reasonably high frequencies ($\leq$ 100 GHz),[5] the equations in

[4]An equivalent circuit is provided in [26] to extract the circuit components from measurement results. However, our work provides a rigorous methodology to analytically calculate the circuit components from geometrical and material properties with better physical insight and can therefore be employed for scaling analysis.

[5]Physically, the inequality comes from the fact that the electromagnetic wavelength is much greater than the TSV height. This is also verified from the calculation results in this and the following sections.

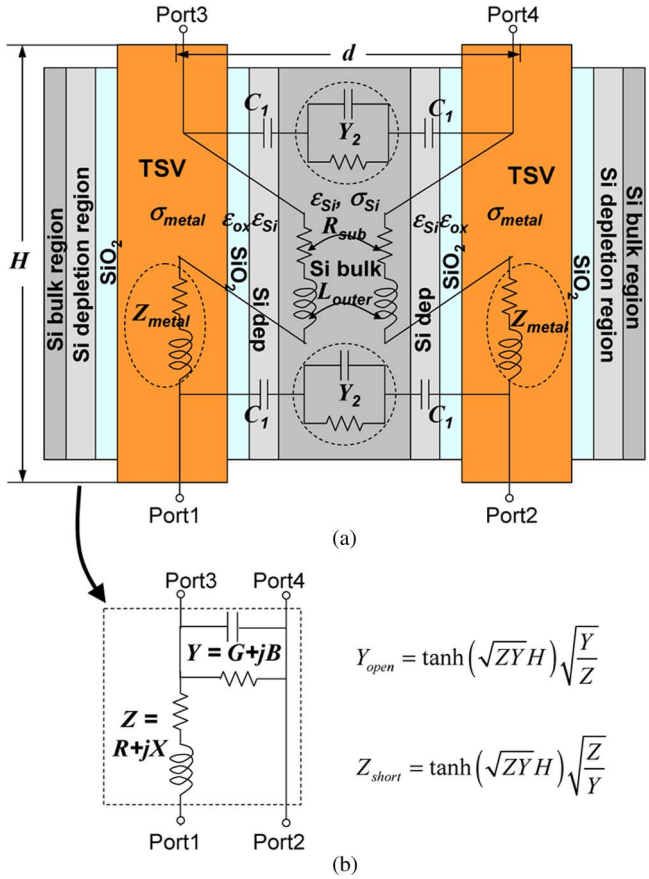

Fig. 5. (a) Equivalent distributed circuit ($RLCG$) model of a pair of TSVs, which can be reduced to (b) a distributed transmission line model. Here, d is the center-to-center distance; $\sigma_{\rm metal}$ and $\sigma_{\rm Si}$ are the conductivity of TSV metal and Si, respectively; C_1 is the capacitance per unit TSV height due to the dielectric and the Si depletion region; Y_2 is the admittance per unit TSV height due to bulk Si; $Z_{\rm metal}$ is the inner impedance per unit TSV height due to the TSV metal; $L_{\rm outer}$ is the outer inductance per unit TSV height between two TSVs; $R_{\rm sub}$ is the resistance per unit TSV height due to eddy currents in the substrate; Y and Z are the effective admittance and the impedance per unit TSV height, respectively; H is the TSV height; and $Y_{\rm open}$ is the input admittance between ports 1 and 2 if ports 3 and 4 are open circuit; similarly, $Z_{\rm short}$ is the input impedance between ports 1 and 2 if ports 3 and 4 are short circuited.

Fig. 5(b) can be reduced to $Y_{\rm open} \approx YH$ and $Z_{\rm short} \approx ZH$, where H is the TSV height.

A. CG Model—Parallel Admittance per TSV Height

The parallel admittance per unit TSV height (Y) can be treated as a series of capacitances of the dielectric and Si depletion region (C_1) and the coupling admittance due to bulk Si (Y_2)

$$Y = \left[2(j\omega C_1)^{-1} + Y_2^{-1}\right]^{-1} = G + j\omega C = G + jB \quad (8)$$

where ω is the radial frequency; the factor of 2 arises from the fact that there are two TSVs and the C_1 of both of them are in series with Y_2, where,

$$C_1 = \left[\frac{1}{2\pi\varepsilon_{\rm ox}} \cdot \ln\left(1 + \frac{t_{\rm ox}}{r_{\rm via}}\right) + \frac{1}{2\pi\varepsilon_{\rm Si}} \cdot \ln\left(1 + \frac{w_{\rm dep}}{r_{\rm via} + t_{\rm ox}}\right)\right]^{-1} \quad (9)$$

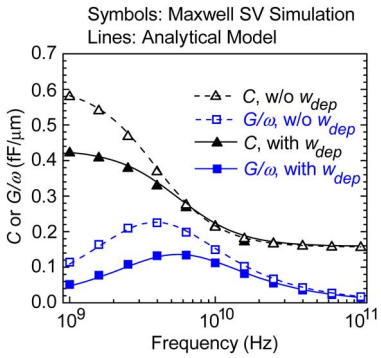

Fig. 6. Parallel admittance (CG) results for a typical pair of TSVs with comparison to Maxwell SV [28] simulation: $d = 15\ \mu$m; $r_{\rm via} = 2.5\ \mu$m; $t_{\rm ox} = 0.5\ \mu$m; $\rho_{\rm Si} = 10\ \Omega$-cm; and $w_{\rm dep} = 0.757\ \mu$m.

which is the same as $C_{\rm MF}$ [see (5)]. Using the method of images [27], one can write

$$Y_2 = \pi(\sigma_{\rm Si} + j\omega\varepsilon_{\rm Si})/\text{arccosh}\left(\frac{d}{2}/(r_{\rm via} + t_{\rm ox} + w_{\rm dep})\right). \tag{10}$$

The calculation result of a typical structure (defined in Fig. 6) agrees well with a 2-D quasi-electrostatic simulation tool Maxwell SV [28]. It can be observed that significant error will be introduced at lower frequencies if the depletion region is not considered, while such error becomes negligible for ultrahigh frequencies. This is because the $j\omega\varepsilon_{\rm Si}$ in the Si depletion region is not very different from the $\sigma_{\rm Si} + j\omega\varepsilon_{\rm Si}$ in the Si bulk region at high frequencies [see (10)], but the difference is significant at low frequencies. Furthermore, at both low frequencies (where $j\omega C_1$ dominates Y) and high frequencies (where $(j\omega C_1)$ and $\text{Im}(Y_2)$ dominate Y), $G/\omega = \text{Re}(Y)/\omega$ is much smaller than $C = \text{Im}(Y)/\omega$, but at about 5.6 GHz, there is a peak for G/ω, implying highest ac conduction (i.e., G is on the same order of C, and is non-negligible).

B. RL Model—Serial Impedance per TSV Height

The serial impedance per unit height (Z) can be expressed as

$$Z = \left(-\frac{d\phi_1}{dz} + \frac{d\phi_2}{dz}\right)/I \tag{11}$$

where ϕ_1 and ϕ_2 are the scalar potentials in TSVs 1 and 2, respectively; I is the total current in the two TSVs. The minus and plus signs in (11) indicate opposite current directions in the two TSVs. In quasi-magnetostatic field [29] (valid because the geometrical parameters in TSVs are much less than 1/4 of the electromagnetic wavelength)

$$-\frac{d\phi}{dz} = E_z + j\omega A_z = \frac{J_z}{\sigma_{\rm eff}} + j\omega A_z \tag{12}$$

where E_z is the z-direction component vertical to the substrate (parallel to the TSV direction) of the electric field in either the TSV metal or the Si substrate; A_z is the corresponding magnetic vector potential; J_z is the corresponding current density; and $\sigma_{\rm eff}$ is the effective conductivity in either the TSV metal or the Si substrate.[6] As shown in (12), both E_z and A_z can be obtained from J_z, which can be treated as the superposition of the impact of the two TSVs (neglecting the proximity effect[7]).

The general differential equation for J_z for a single-TSV azimuthal system can be obtained from Maxwell's equations (for example, see [22]), i.e.,

$$j\omega\mu J_z(r) = \frac{1}{r}\cdot\frac{d}{dr}\left(r\cdot\frac{d}{dr}E_z(r)\right) = \frac{1}{\sigma_{\rm eff}}\cdot\frac{1}{r}\cdot\frac{d}{dr}\left(r\cdot\frac{d}{dr}J_z(r)\right) \tag{13}$$

where μ is the permeability in either the TSV metal or Si (usually very close to the value in vacuum); and r is the radial direction coordinate of TSV.

In the case of a single TSV, the boundary conditions require that $J_z(0)$ has a finite value while $J_z(\infty) = 0$. Consequently, the expression for $J_z(r)$ can be written as

$$J_z(r) = \begin{cases} c_1 \text{J}_0\left((1-j)r/\delta_{\rm metal}\right), & r < r_{\rm via} \\ c_2 \text{H}_0^{(2)}\left((1-j)r/\delta_{\rm Si}\right), & r > r_{\rm via} + t_{\rm ox} + w_{\rm dep} \end{cases} \tag{14}$$

where c_1 and c_2 are constants; J_0 is the 0th order Bessel function of the first type; $\text{H}_0^{(2)}$ is the 0th order Hankel function of the second type; and $\delta_{\rm metal}$ and $\delta_{\rm Si}$ are the damping parameters, i.e.,

$$\delta_{\rm metal} = \sqrt{2/\omega\mu\sigma_{\rm metal}} \quad \delta_{\rm Si} = \sqrt{2/\omega\mu\left(\sigma_{\rm Si} + j\omega\varepsilon_{\rm Si}\right)}. \tag{15}$$

c_1 and c_2 can be normalized as

$$\frac{c_1}{I} = \left[\int_0^{r_{\rm via}} \text{J}_0\left((1-j)r/\delta_{\rm metal}\right)\cdot 2\pi r dr\right]^{-1}$$
$$= (1-j)\left[2\pi r_{\rm via}\delta_{\rm metal}\text{J}_1\left((1-j)r_{\rm via}/\delta_{\rm metal}\right)\right]^{-1} \tag{16a}$$

$$\frac{c_2}{I} = -\left[\int_{r_{\rm via}+t_{\rm ox}+w_{\rm dep}}^{\infty} \text{H}_0^{(2)}\left((1-j)r/\delta_{\rm Si}\right)\cdot 2\pi r dr\right]^{-1}$$
$$= \frac{\left[(1+j)\pi\cdot\delta_{\rm Si}\cdot(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right]^{-1}}{\text{H}_1^{(2)}((1-j)(r_{\rm via}+t_{\rm ox}+w_{\rm dep})/\delta_{\rm Si})} \approx -\frac{1}{2\delta_{\rm Si}^2} \tag{16b}$$

where I is the total current; J_1 is the 1st order Bessel function of the first type; $\text{H}_1^{(2)}$ is the 1st order Hankel function of the second type; the equivalence sign is valid since $r_{\rm via}+t_{\rm ox}+w_{\rm dep} << \delta_{\rm Si}$.

From (11), (12), and the superposition of two TSVs, $d\phi/dz$ in the two TSVs can be expressed as

$$-\frac{1}{I}\cdot\frac{d\phi_1}{dz} = \frac{1}{I}\cdot\frac{d\phi_2}{dz} \approx \frac{J_z(r_{\rm via}-\Delta r)}{\sigma_{\rm metal}I} + \frac{j\omega}{I}\left[A_z(r_{\rm via}) - A_z(d)\right]$$
$$= J_z(r_{\rm via}-\Delta r)/(\sigma_{\rm metal}I) + (j\omega/I)\left[A_z(r_{\rm via}) - A_z(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right] + (j\omega/I)\left[A_z(r_{\rm via}+t_{\rm ox}+w_{\rm dep}) - A_z(d)\right] \tag{17}$$

[6]In traditional metals (Cu, W, etc.), $\sigma_{\rm eff}$ is just the dc conductivity; in Si, $\sigma_{\rm eff,Si} = \sigma_{\rm Si} + j\omega\varepsilon_{\rm Si}$, where $\sigma_{\rm Si}$ is the dc conductivity of Si and $\varepsilon_{\rm Si}$ is the permittivity of Si; and $\sigma_{\rm eff}$ in CNTs should take kinetic inductance and quantum conductance into account, which will be explained in the next section.

[7]The proximity effect is not important because the center-to-center distance between TSVs is usually more than six times the radius of TSVs. This is confirmed by comparing the calculation results with the Maxwell SV(Fig. 7).

where Δr is an infinitesimal value; and $J_z(r_{\rm via}-\Delta r)$ indicates the current density at the surface of the TSV metal. According to (14) and (16a), the first term on the right-hand side of (17), called the inner impedance $(Z_{\rm metal})$, can be expressed as

$$Z_{\rm metal}=\frac{J_z(r_{\rm via}-\Delta r)}{\sigma_{\rm metal}I}=\frac{(1-j)\cdot \mathrm{J}_0\left((1-j)r_{\rm via}/\delta_{\rm metal}\right)}{\sigma_{\rm metal}\cdot 2\pi r_{\rm via}\delta_{\rm metal}\cdot \mathrm{J}_1\left((1-j)r_{\rm via}/\delta_{\rm metal}\right)}. \tag{18}$$

The second term on the right-hand side of (17) is purely imaginary, which can be obtained from the vector potential Green's function as:

$$\frac{j\omega}{I}\left[A_z(r_{\rm via})-A_z(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right]=\frac{j\omega\mu}{2\pi}\cdot\ln\left(\frac{r_{\rm via}+t_{\rm ox}+w_{\rm dep}}{r_{\rm via}}\right). \tag{19}$$

Since the $d\phi/dz$ outside the two TSVs is zero, the third term on the right-hand side of (17) can be derived from (14)–(16b), i.e.,

$$\begin{aligned}&\frac{j\omega\left[A_z(r_{\rm via}+t_{\rm ox}+w_{\rm dep})-A_z(d)\right]}{I}\\&=\frac{-J_z(r_{\rm via}+t_{\rm ox}+w_{\rm dep}+\Delta r)+J_z(d)}{(\sigma_{\rm Si}+j\omega\varepsilon_{\rm Si})I}\\&\approx\frac{\omega\mu}{4}\left[\mathrm{H}_0^{(2)}\left(\frac{1-j}{\delta_{\rm Si}}(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right)-\mathrm{H}_0^{(2)}\left(\frac{(1-j)d}{\delta_{\rm Si}}\right)\right].\end{aligned} \tag{20}$$

The real part of this term is physically due to the eddy current. Multiplying by 2 (due to 2 TSVs),

$$R_{\rm sub}\approx\frac{\omega\mu}{2}\cdot\mathrm{Re}\left[\mathrm{H}_0^{(2)}\left(\frac{1-j}{\delta_{\rm Si}}(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right)-\mathrm{H}_0^{(2)}\left(\frac{(1-j)d}{\delta_{\rm Si}}\right)\right]. \tag{21}$$

Multiplying the sum of the right-hand side of (19) and the imaginary part of the right-hand side of (20) by 2 gives $\omega L_{\rm outer}$ (where $L_{\rm outer}$ is the outer inductance):

$$\begin{aligned}L_{\rm outer}\approx&\frac{\mu}{\pi}\ln\left(\frac{r_{\rm via}+t_{\rm ox}+w_{\rm dep}}{r_{\rm via}}\right)\\&+\frac{\mu}{2}\cdot\mathrm{Im}\left[\mathrm{H}_0^{(2)}\left(\frac{1-j}{\delta_{\rm Si}}(r_{\rm via}+t_{\rm ox}+w_{\rm dep})\right)-\mathrm{H}_0^{(2)}\left(\frac{(1-j)d}{\delta_{\rm Si}}\right)\right].\end{aligned} \tag{22}$$

Therefore, the serial impedance per unit height (Z) can be treated as the sum of three components, i.e., the inner impedance of the TSV $(Z_{\rm metal})$, the outer inductance $(L_{\rm outer})$, and the resistance due to eddy current in the substrate $(R_{\rm sub})$, i.e.,

$$Z=2Z_{\rm metal}+j\omega L_{\rm outer}+R_{\rm sub}. \tag{23}$$

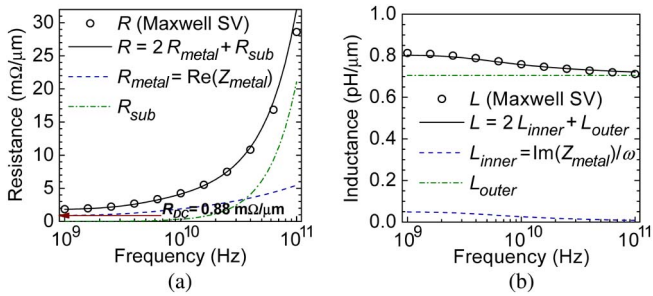

Fig. 7. Serial impedance (RL) calculation results (lines) compared with Maxwell SV [28] simulation (symbols) for a typical pair of TSVs: (a) resistance versus frequency and (b) inductance versus frequency. The via metal is assumed to be Cu (1.7 $\mu\Omega$-cm); $\rho_{\rm Si}=0.1$ Ω-cm; $w_{\rm dep}=43.6$ nm;[8] and all the other parameters are the same as in Fig. 6.

In the case of a TSV pair where one TSV serves as the return path of the other, $L_{\rm outer}$ is approximately the reciprocal of the "capacitance" between two TSVs as if the "medium permittivity" between the TSVs is $1/\mu$. This is valid as long as $|\delta_{\rm Si}|\gg d$. Similar to (10), $L_{\rm outer}$ can also be expressed as

$$L_{\rm outer}\approx\frac{\mu}{\pi}\mathrm{arccosh}\left(\frac{d}{2r_{\rm via}}\right). \tag{24}$$

In the following analysis, (24) is used to calculate $L_{\rm outer}$.

The calculation result of a typical structure (shown in Fig. 7) agrees well with a 2-D quasi-magnetostatic simulation tool Maxwell SV [28]. The results indicate that the skin effect in TSV metals is important for high-frequency analysis, while dc resistance is much smaller than high-frequency resistance.

C. Verification of RLCG Model With Full-Wave Simulation

The $RLCG$ model presented here is benchmarked with a commercial full-wave electromagnetic (EM) simulation tool (HFSS v.10 [30]) by comparing the results for open-circuit admittance $(Y_{\rm open})$ and the short-circuit impedance $(Z_{\rm short})$. According to the transmission line theory

$$Y_{\rm open}=\tanh(\sqrt{ZY}H)\sqrt{Y/Z} \tag{25}$$

$$Z_{\rm short}=\tanh(\sqrt{ZY}H)\sqrt{Z/Y}. \tag{26}$$

Note that Z and Y are the impedance and admittance per unit TSV height, respectively, as calculated in (8) and (23). The comparison results are shown in Fig. 8. The calculated $Y_{\rm open}$ values are in excellent agreement with those of HFSS. However, there is a deviation for $Z_{\rm short}$. This is due to the inaccuracy of 2-D approximation in RL modeling of real 3-D configurations (the 2-D approximation is valid when $d<<H$). However, the real and imaginary parts of $Z_{\rm short}$ are very small, implying that both R and L are very small. Hence, our approximation has very little impact on the performance analysis when we include active devices (as shown in the last section).

[8] $\rho_{\rm Si}=0.1$ Ω-cm instead of 10 Ω-cm is used in Fig. 7 to demonstrate the accuracy of $R_{\rm sub}$ (resistance due to the eddy current). $w_{\rm dep}=43.6$ nm is calculated by assuming $Q_i/q=5\times10^{11}$ cm^{-2} and a bias voltage of 0.6 V.

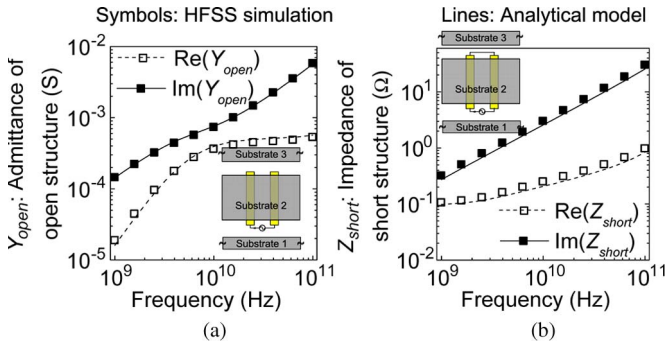

Fig. 8. Calculation result for (a) open and (b) short structures of Fig. 5(a) and the comparison with HFSS [30] (insets show the schematic of the structure). The TSV height is 54 μm; the thickness of silicon substrate 2 is 50 μm; SiO_2 is filled between the substrates, which are separated by 12 μm; via metal is assumed to be Cu (1.7 $\mu\Omega$-cm); and all the other parameters are the same as in Fig. 6. To extract $Y_{\rm open}$ and $Z_{\rm short}$ in HFSS, two lumped ports are applied at both the bottom (ports 1 and 2) and top (ports 3 and 4) of the TSV pair, which form a two-port network: $Y_{\rm open} = 1/Z_{11}$ and $Z_{\rm short} = 1/Y_{11}$. Y_{11} is the current flowing out of port 1 divided by the voltage difference between ports 1 and 2, when the voltage difference between ports 3 and 4 is artificially made to be zero.

IV. RL Model for CNT TSVs

Given that the CG model for different TSV materials is identical,[9] we focus on the different behavior of the RL model for CNT TSVs. As stated in [21] and [22], using an "effective dc conductivity" in CNTs leads to significant error in high-frequency impedance analysis, which is due to the kinetic-inductance-induced reduction in skin effect; a "complex effective conductivity" $(\sigma_{\rm eff})$ should be used to take this into account. $\sigma_{\rm eff}$ can be derived from the intrinsic self impedance of an isolated single-walled CNT (SWCNT) or an individual shell of a multiwalled CNT (MWCNT) $(Z_{\rm CNT,self})$ [22], i.e.,

$$Z_{\rm CNT,self} = \frac{R_{\rm mc} + R_Q + R_S + j\omega L_K}{N} = \frac{h}{2q^2 N}\left(1 + \frac{H}{\lambda} + j\omega\frac{H}{2v_F}\right) + \frac{R_{\rm mc}}{N} \quad (27)$$

where $R_{\rm mc}$, R_Q, R_S, and L_K are the imperfect contact resistance,[10] the quantum contact resistance, the scattering resistance, and the kinetic inductance of each conducting channel, respectively; H is the TSV height; N is the number of conducting channels in an SWCNT or a shell of an MWCNT; h is Planck's constant; $v_F = 8 \times 10^5$ m/s is the Fermi velocity; and λ is the electron MFP, which can be expressed as [21], [22]

$$\lambda = 1000D \quad (28)$$

where D is the diameter of the corresponding SWCNT or the shell of an MWCNT. For SWCNT bundles, the effective value of N is dependent on the metallic fraction (Fm). $N = 2$ if all CNTs are metallic $(Fm = 1)$, while an effective value of $N =$ 2/3, if 1/3 of the CNTs in the bundle are metallic $(Fm = 1/3)$. It should be noted that SWCNTs with very high metallic fraction $(Fm = 0.91)$ have already been achieved [31]. For MWCNTs, the number of conducting channels for a given shell [32]

$$N \approx 0.0612D + 0.425 \quad (29)$$

where D is expressed in nanometers. Assuming that the CNTs are closely packed (the gap between CNTs $s = 0.34$ nm, as shown in Fig. 9), $\sigma_{\rm eff}$ can be obtained. For the SWCNT bundle, $\sigma_{\rm eff}$ can be expressed as

$$\sigma_{\rm eff} = H\left[\frac{\sqrt{3}}{2}(D+s)^2 Z_{\rm CNT,self}\right]^{-1}. \quad (30)$$

For the MWCNT bundle

$$\sigma_{\rm eff} = H \cdot \frac{2}{\sqrt{3}}(D_{\rm out}+s)^{-2} \cdot \sum_{\rm shell} Z_{\rm CNT,self}^{-1} \quad (31)$$

where $D_{\rm out}$ is the diameter of the outmost shell of a MWCNT. For the RL calculation of CNT based TSVs, one can replace $\sigma_{\rm metal}$ in (15) and (18) with $\sigma_{\rm eff}$ from (30) or (31) to calculate $Z_{\rm metal}$, while the calculations for $R_{\rm sub}$, $L_{\rm outer}$ and Z remain the same as in (21)–(24).

Using the "complex effective conductivity" approach, the impedance for a pair of TSVs can be obtained and is compared with those of Cu and W. According to Fig. 10, the MWCNT-based TSVs offer almost the same low-frequency resistance as Cu but have a much lower high-frequency resistance than Cu due to reduced skin effects [21], [22]. For SWCNTs (1/3 metallic), the resistance is greater than that of Cu for frequencies

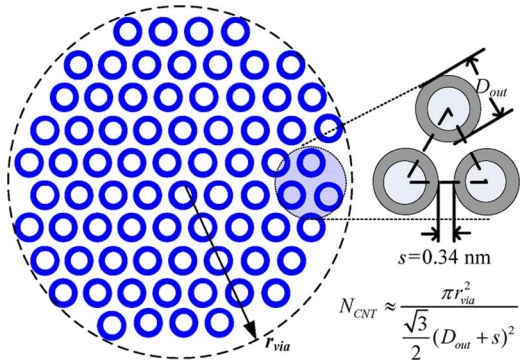

Fig. 9. Cross-sectional view of a closely packed CNT bundle used as TSV metal. N_{CNT} is the total number of CNTs in the bundle.

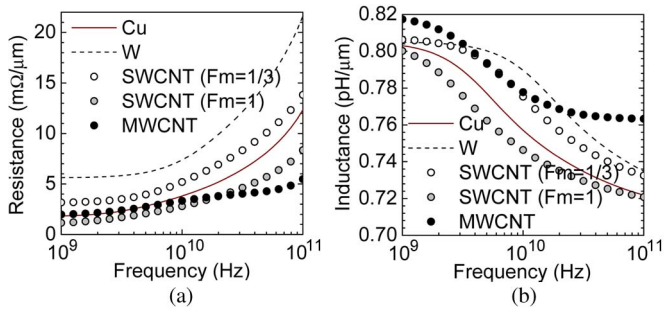

Fig. 10. Impedance (RL) results of Cu, W (5.3 $\mu\Omega$-cm), SWCNT bundle, and MWCNT bundle for a typical pair of TSVs: (a) resistance versus frequency and (b) inductance versus frequency. Fm denotes the fraction of metallic SWCNTs in the bundle. SWCNTs are assumed to have a diameter of 1 nm. The MWCNTs are assumed to have an outmost diameter of 20 nm. The TSV height is assumed to be 54 μm. All the other parameters are the same as in Fig. 8.

[9]For CNT-based TSVs, the number of CNTs is still large enough so that the quantum capacitance can be ignored.

[10]The imperfect contact resistance is highly process dependent. In this paper, we consider the ideal case, i.e., $R_{\rm mc}$ is 0.

TABLE I
TSV GEOMETRICAL PARAMETERS BASED ON ITRS'08 [33]

Year	2009	2010	2011	2012	2013	2014	2015
Technology node	32 nm			22 nm			
Radius r_{via} (μm)	0.75	0.71	0.67	0.63	0.59	0.56	0.52
Minimum (ITRS) pitch d_{min} (μm)	5.51	4.42	3.83	3.76	2.68	2.61	2.55
Pitch taken in this work d (μm)	8.26	6.63	5.75	5.63	4.02	3.92	3.82
Height H (μm) *	20	20	20	20	20	20	20
Oxide thickness t_{ox} (μm) **	0.151	0.142	0.133	0.126	0.118	0.111	0.105
Depletion width w_{dep} (μm) ***	0.711	0.708	0.705	0.701	0.698	0.695	0.691

* According to ITRS, the minimum thickness of Si substrate is 10 μm. However, nominal thickness is larger to allow for the variation; also, the TSV height should be greater than substrate thickness.
** There is no value of t_{ox} in ITRS. t_{ox} is assumed to be $r_{via}/5$.
*** w_{dep} is calculated by assuming a p-type Si substrate and $\rho_{Si} = 10$ Ω-cm.

below 100 GHz, while the difference decreases as the frequency increases. Furthermore, as expected, the resistance of W TSV is the highest. The resistances of SWCNTs (all metallic) and MWCNTs are the lowest at the lower and higher frequencies, respectively. The inductances of Cu, W, SWCNT, and MWCNT TSVs are almost identical, since it is the outer inductance rather than inner inductance that dominates.

V. SCALING ANALYSIS OF TSVS

The International Technology Roadmap for Semiconductors (ITRS) [33] provides scaling predictions for TSV geometries (Table I). As technology scales, both the radius and pitch of TSVs reduce, while the substrate thickness (determining the TSV height) remains same.

From Table I and the analytical models presented earlier, the $RLCG$ of a TSV pair (per unit TSV height) is computed, and the results are shown in Fig. 11. As technology scales, C, G, and L do not change very much because the geometrical parameters scale nearly proportionally; R increases a lot at 1 GHz, as well as at 100 GHz. This is due to the decreasing area and perimeter of the TSV cross section. From the resistance perspective, MWCNT is worse than Cu at 1 GHz [Fig. 11(c)]. Although MWCNTs have advantages over Cu at higher frequencies, the benefits diminish as technology scales [Fig. 11(d)]. This is not in conflict with Fig. 10(a), because the geometrical dimension of the TSVs in Fig. 11 is much smaller: a smaller radius results in a lower skin effect in Cu, while a shorter height implies a higher effective resistivity of MWCNT due to the quantum contact resistance [34]. Furthermore, the total inductance of MWCNT becomes apparently greater than that of other materials, because a smaller cross-sectional area indicates a greater ratio of kinetic inductance to total inductance [21], [22]. On the other hand, the SWCNT bundle (all metallic) maintains its advantage over Cu, since their electrical MFP is much smaller than the TSV height.

VI. ELECTRICAL PERFORMANCE OF TSVS

The 3-D ICs require both power/ground and signal TSVs to communicate with the components on different substrates. The power/ground TSVs and horizontal wires are usually periodically placed, forming the power/ground grid [35]. For performance analysis, each power/ground TSV can be treated as the ac ground and current return path shared by several signal TSVs. In a simple situation, one V_{DD} TSV, one GND TSV, and one signal TSV with the inverters (driver and load) on different substrates form a circuit network, as shown in Fig. 12. The parallel admittance network and serial impedance network of the 3-TSV system are illustrated and verified in Fig. 12(a)–(d). The parameters in the 3-TSV system can be obtained from the TSV pairs. In particular, in the network of parallel admittance, the capacitance C_1 is still the same as that illustrated in Fig. 5(a) and can be expressed as in (9); while the admittance $Y_{2,\mathrm{VS}}$, $Y_{2,\mathrm{SG}}$, and $Y_{2,\mathrm{VG}}$ can be obtained from

$$\begin{cases} Y_2(d=d_0) = Y_{2,\mathrm{VS}} + \left(Y_{2,\mathrm{SG}}^{-1} + Y_{2,\mathrm{VG}}^{-1}\right)^{-1} \\ Y_2(d=2d_0) = Y_{2,\mathrm{VG}} + \left(Y_{2,\mathrm{VS}}^{-1} + Y_{2,\mathrm{SG}}^{-1}\right)^{-1} \\ Y_{2,\mathrm{VS}} = Y_{2,\mathrm{SG}} \end{cases} \tag{32}$$

where Y_2 is a function of the center-to-center distance (d) of a TSV pair, given in (10). For the TSV pair of V_{DD}–signal or signal–GND, $d = d_0$. For that of V_{DD}–GND, $d = 2d_0$. In the network of serial impedance

$$\begin{cases} Z_V = Z_S = Z_G = Z(d=d_0)/2 \\ j\omega M_{\mathrm{VG}} = \left[Z(d=d_0) - Z(d=2d_0)\right]/2 \end{cases} \tag{33}$$

where Z is a function of d of a TSV pair, given in (23); and $j\omega M_{\mathrm{VG}}$ is the mutual impedance (for a low-conductivity substrate, as discussed in this paper, the real part of $j\omega M_{\mathrm{VG}}$ can be ignored). Incorporating these networks into the inverter-based driver–receiver circuit [Fig. 12(e)], the performance (delay, rise/fall time, etc.) can be analyzed.

The performance of Cu-, W-, SWCNT-bundle, and MWCNT-bundle-based TSVs at 22-nm technology node is compared for different driver sizes (Fig. 13). As the inverter size increases, the delay and rise times of the signal voltage decrease, as expected. On the other hand, the delay does not quite depend on the TSV material, although there is a significant difference in resistance and some difference in inductance among those materials. This result is different from long-horizontal-wire analysis, where metal resistance dramatically affects the performance since it is mostly RC dominated.

By changing the values of either C, G, R, or L, the sensitivity to the $RLCG$ parameters of the circuit performance can be obtained [Fig. 14(a) and (b)]. The figure indicates that the capacitance is the most important parameter, because a 5% error in capacitance leads to up to 2.4% error in the delay and 2.6% error in the rise time of the signal voltage. On the other hand, for any reasonable inverter sizes (below 300 times the minimum size), the resistance is the least important parameter, because a 20% error in resistance only leads to up to 0.17% error in the delay and 0.35% error in the rise time of the signal voltage. The importance of conductance and inductance is somewhere in between. This is a clear indication of the short-transmission-line behavior of the signal propagation. In other words, for the typical TSV sizes, the attenuation would not be a big concern (G is not as important as C, while R is not as important as L). On the other hand, at least for digital applications with reasonable driver sizes, our compact $RLCG$ model is sufficient for performance analysis, since it has good accuracy for CG

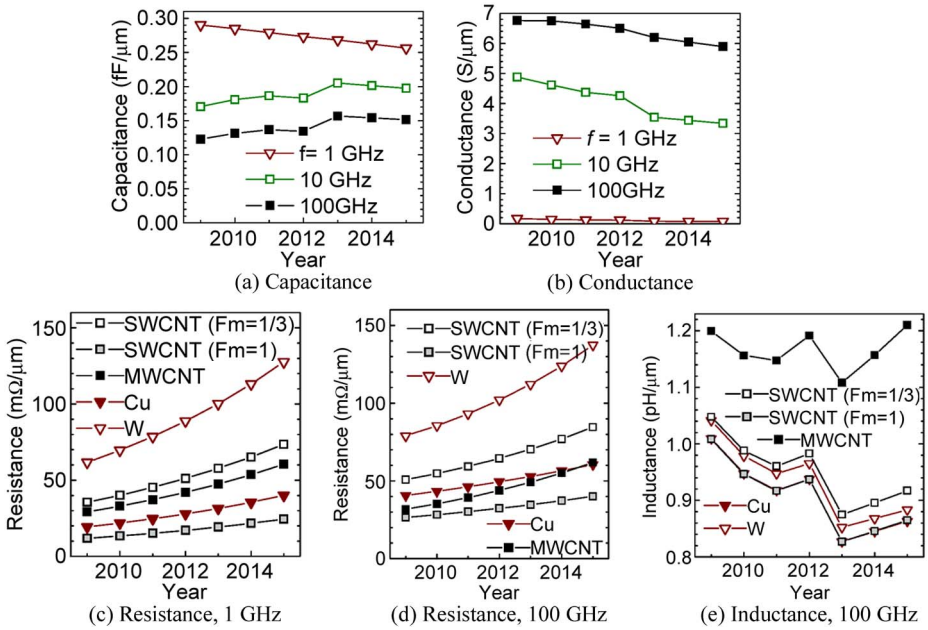

Fig. 11. Scaling analysis of the $RLCG$ of the TSV pair according to ITRS: (a) capacitance ($C = \mathrm{Im}(Y)/\omega$) (all of them are shown as per unit TSV height); (b) conductance ($G = \mathrm{Re}(Y)$); (c) resistance ($R = \mathrm{Re}(Z)$) for $f = 1$ GHz; (d) resistance ($R = \mathrm{Re}(Z)$) for $f = 100$ GHz; and (e) inductance ($L = \mathrm{Im}(Z)/\omega$) for $f = 100$ GHz (note that the data points for SWCNT ($Fm = 1$) and Cu almost coincide). The geometrical parameters are from Table I, while all the material properties are the same as in Fig. 10. Note that C and G in (a) and (b) are independent of TSV metal. Furthermore, the quantum capacitance for the CNT bundle is extremely large as compared to the electrostatic component, which implies that its effect can be ignored.

extractions. It should be noted that although the inductance is not that critically important in delay and rise time calculations, it is crucial in the estimation of voltage variations in $\mathrm{V_{DD}}$ and GND lines [Fig. 14(c)]: purely assuming an RC circuit (blue dashed curve) is insufficient. The inductance extraction can further be used in decoupling capacitance design.

VII. Thermal Performance of TSVs

The previous section indicates that difference among different TSV metals only has negligible ($< 1\%$) effect on circuit performance. On the other hand, it is known that W has a much lower thermal conductivity than Cu, while both the SWCNT and MWCNT bundles can have a much greater thermal conductivity than Cu [23], [37]. Therefore, it is also important to examine the thermal performance of TSVs. In particular, the TSVs themselves produce only negligible Joule heating as compared to the active regions on top of the silicon surface. This is trivially explained by the much smaller resistance of TSVs compared with the resistance of active devices. However, the heat conduction by TSVs can be crucial in reducing the temperature increase in the upper layers of 3-D ICs.

A schematic simulation structure is shown in Fig. 15(a). The geometrical parameters of TSVs (pitch, radius, and isolation oxide thickness) are chosen from Table I (22-nm technology node, Year 2013). Using the mirror symmetry property, the periodic TSV distribution is simplified as a half TSV with the surrounding cross-sectional area of pitch $\times$ pitch/2 in the XOY plane.

Both the lower and upper chips have back-end-of-line (BEOL) layers of total thickness $= 3$ μm. The BEOL layer is treated as an equivalent medium with anisotropic effective thermal conductivity ($\kappa_z = 2$ W/(m $\cdot$ K); $\kappa_x = \kappa_y = 25$ W/(m $\cdot$ K). The higher thermal conductivity in the horizontal direction is due to the larger density of horizontal wires than that of vertical short vias) [38]. Between the two chips, there is 0.7-μm region of air, which is required in the via-first thermo-compression bonding process [6]. The TSV is between the top global interconnect in the lower chip and metal 1 in the upper chip. Both pads are assumed to be made of Cu. A Cu stud is added between the top global wire pad and metal 1 in the lower chip to be treated as thermal dissipation via. Only the TSV itself is changed from Cu to W and CNT bundle. The total height from metal 1 in the lower chip to that in the upper chip is 20 μm. The TSV is treated as a thermal dissipation path, while the silicon surface, where the active region lies, is treated as the heat source, assuming a 100 W/cm^2 power density for the entire upper chip or 111 W/cm^2 on the silicon surface (excluding the area of the TSV).

To evaluate the thermal benefit from CNTs, the thermal conductivity of the CNT bundle needs to be examined. In [39], a range of 1750–5800 W/(m $\cdot$ K) (according to [23]) is assumed in the analysis of SWCNT short vias. However, as pointed out in [25], this assumption is not quite valid for short vias, since the height of short vias is generally smaller than the phonon MFP ($\sim\mu$m). Instead, [25] assumes a ballistic constant thermal conductance for different via heights.

On the other hand, for TSVs, the height is usually much larger than the phonon MFP, implying that a range of 1750–5800 W/(m $\cdot$ K) is valid for the analysis of TSVs. In addition to the thermal conductivity along CNTs (z-direction), the perpendicular thermal conductivity should also be included. In this paper, the air thermal conductivity (0.024 W/(m $\cdot$ K)) is used as the lower bound, while the c-axis thermal conductivity of bulk graphite ($\sim$10 W/(m $\cdot$ K) [40]) is used as the upper bound. Medium values of the thermal

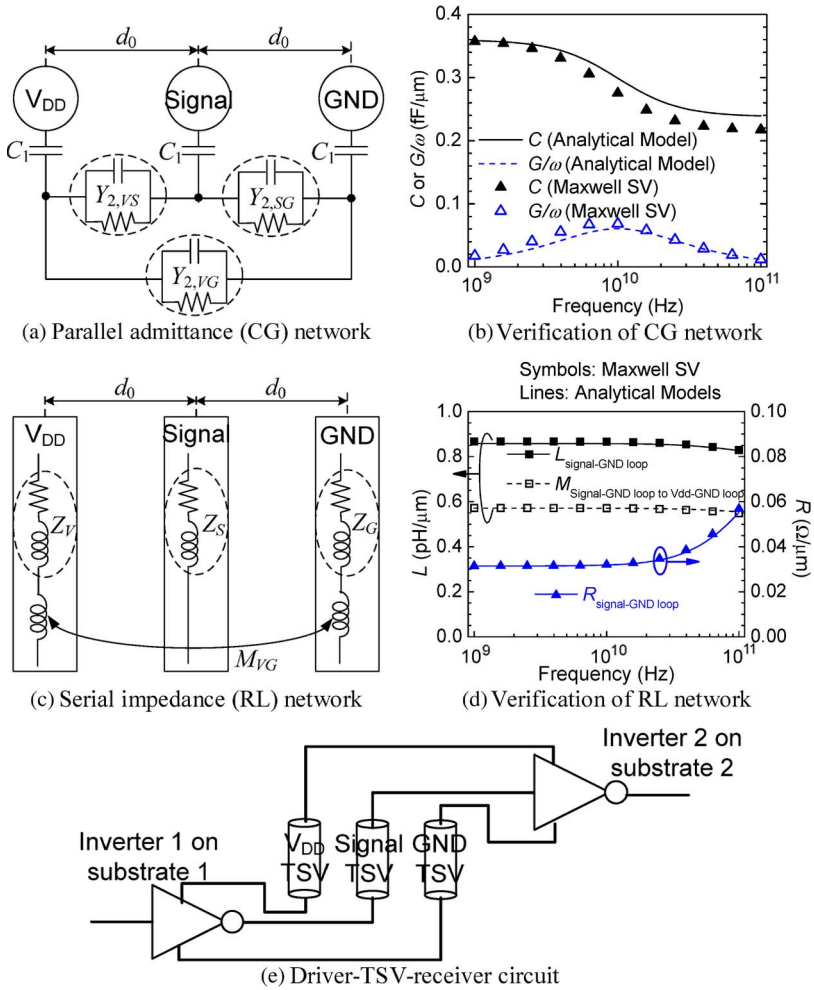

Fig. 12. (a) Equivalent parallel admittance (CG) network of a three-TSV system (with V_{DD}, signal, and GND TSVs) and (b) its verification against Maxwell SV [28]; (c) equivalent serial impedance (RL) network of the three-TSV system and (d) its verification against Maxwell SV; the networks can be incorporated into (e) the driver–TSV–receiver circuit. In (b) and (d), the geometrical parameters are from Table I (22-nm technology node, Year 2013). In (b), $\rho_{Si} = 10\ \Omega$-cm, and $w_{dep} = 698$ nm; the data represent the total C and G/ω of the signal TSV with respect to the GND/V_{DD} TSVs with ac shorted GND and V_{DD}. In (d), $\rho_{Si} = 0.1\ \Omega$-cm, and $w_{dep} = 51.3$ nm; the data represent the self-inductance and resistance of the signal–GND loop and the mutual inductance of the signal–GND loop to the V_{DD}–GND loop.

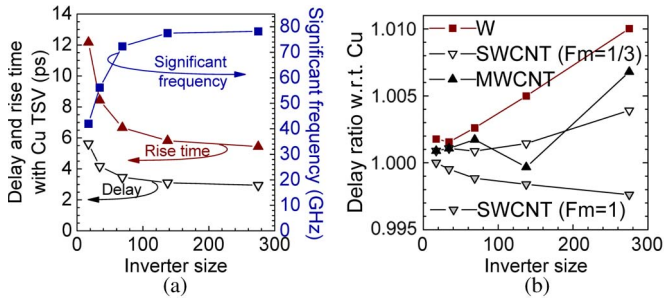

Fig. 13. Performance analysis of inverters driving the same sized inverters of 22-nm technology node with TSVs connected between them: (a) average delay and rise time of the signal voltage and significant frequency (f_B) of the circuit with Cu TSVs; and (b) delay ratio w.r.t. Cu TSVs for other materials. f_B is obtained from the rise/fall time of transition current; the resistance and inductance are assumed to have the value at f_B. The geometrical parameters are from Table I (Year 2013), while all material properties are the same as in Fig. 10. The inverter sizes shown are normalized values (as in [18]) w.r.t. a minimum sized 2:1 inverter with the width of NMOS = 32 nm. The device model is from PTM [36].

conductivities employ $\kappa_z = 3000\ \mathrm{W/(m \cdot K)}$ from the MWCNT in [37] and $\kappa_x = \kappa_y = 0.1\ \mathrm{W/(m \cdot K)}$. A typical temperature profile of a two-layer 3-D chip embedding a CNT TSV with medium values of thermal conductivities is shown in Fig. 15(b).

The results are summarized in Table II. The CNT bundle TSV shows better thermal dissipation (lower maximum temperature rise) than the Cu TSV, even if a pessimistic thermal conductivity ($\kappa_z = 1750\ \mathrm{W/(m \cdot K)}$, $\kappa_x = \kappa_y = 0.024\ \mathrm{W/(m \cdot K)}$) of the CNT bundle is assumed. Furthermore, as expected, W shows the worst thermal dissipation, having the highest temperature rise. It should be noted that the maximum temperature rise in the system is not inversely proportional to the thermal conductivity of the TSV metal. This is due to the fact that the thermal dissipation in Si substrate, as well as in the BEOL layer and Cu stud, also contributes to the temperature rise. Furthermore, the readers may note that the temperature rise in Table II, irrespective of the TSV metal assumed, is not very high. However, the temperature rise depends on the power consumption and distance to the lowest Si substrate (when more than two chips are stacked together) [42], as well as the TSV density (related to the distance between TSVs). The temperature versus the x-directional center-to-center distance of TSVs (d_x) is shown in Fig. 16. Temperature rise of several

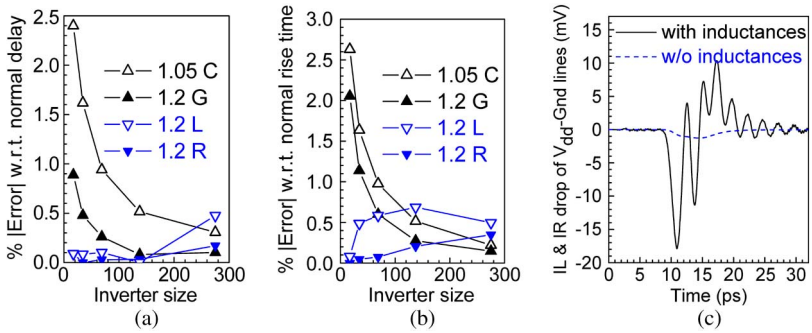

Fig. 14. Impact of the inaccuracy of the C, G, R, and L of the TSVs on the inaccuracy of the (a) delay and (b) rise time of the signal voltage. For example, the curve "1.05 C" in (a) indicates % |Error| of delay w.r.t. Fig. 13(a) if the TSV capacitances are assumed to be 1.05 times the value in Fig. 13(a), while all the other parameters, device models, and simulation method are the same as in Fig. 13(a). (c) Impact of the L of the TSVs on the V_{DD}/GND noise (IL & IR drop) during the switching of an inverter (the inverter size is 69, and no decoupling capacitance between V_{DD} and GND is assumed in the simulation).

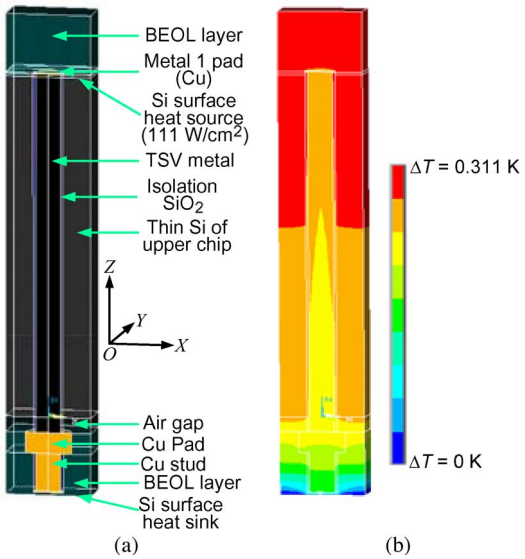

Fig. 15. Thermal simulation of a 3-D structure with two stacked Si chips connected with TSVs, assuming a via-first thermo-compression bonding process [6]: (a) the simulated structure using the mirror symmetry property; (b) temperature profile (the temperature rise is with respect to the Si surface of lower chip) with CNT as the TSV metal ($\kappa_z = 3000$ W/(m · K) [37]; $\kappa_x = \kappa_y = 0.1$ W/(m · K)). The simulation is performed by a finite-element method (FEM)-based software, ANSYS Multiphyiscs [41].

TABLE II
THERMAL SIMULATION RESULTS OF THE STRUCTURE IN FIG. 15(a)

TSV metal	Thermal conductivity	Maximum temperature rise
Cu	390 W/(m·K)	0.434 K
W	173 W/(m·K)	0.535 K
CNT (less optimistic assumption)	κ_z = 1750 W/(m·K) $\kappa_x = \kappa_y$ = 0.024 W/(m·K)	0.337 K
CNT (more optimistic assumption)	κ_z = 5800 W/(m·K) $\kappa_x = \kappa_y$ = 10 W/(m·K)	0.289 K
CNT (medium assumption)	κ_z = 3000 W/(m·K) $\kappa_x = \kappa_y$ = 0.1 W/(m·K)	0.311 K

degree Kelvin can be observed if the distance between TSVs increases. On the other hand, when d_x becomes large, the heat dissipation through the polymer glue layer [in Fig. 16(b)] starts to contribute, and the difference among CNT, Cu, and W shrinks.

In summary, the thermal issue can become non-negligible or even crucial as the power density and the number of stacked

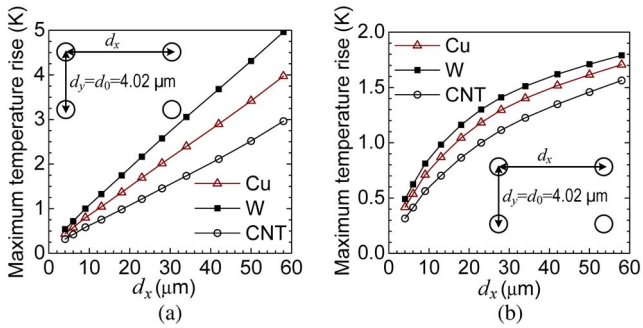

Fig. 16. Maximum temperature in the structure shown in Fig. 15(a) as a function of the center-to-center distance in the x-direction (d_x) (schematic top view shown in the insets) for different types of TSV metals, assuming (a) an air gap (as in [6]) and (b) polymer glue (as in [8], $\kappa_{\text{glue}} = 1$ W/(m · K)) between chips. The center-to-center distance in the y-direction (d_y) is kept at 4.02 μm. For the data labeled "CNT," the thermal conductivity of medium assumption (see Table II) is used. All the other geometrical and material properties are the same as in Fig. 15. The simulations are performed by an FEM-based software, ANSYS Multiphyiscs [41].

chips increases. CNTs, with a much higher thermal conductivity than Cu and W, can be beneficial from a thermal point of view.

VIII. CONCLUSION

Accurate electrostatic and high-frequency $RLCG$ compact models for TSVs needed in 3-D ICs have been developed. The electrostatic model has been validated against both measurements and simulations. The results have shown that the MOS effect or the depletion region surrounding the TSV isolation dielectric must be considered for accurate ac analysis. Both CG and RL models have been verified against a 2-D quasi-electrostatic and quasi-magnetostatic simulator (Maxwell SV). Combining the CG and RL models and the transmission line model, the admittance/impedance of a TSV pair can be obtained, which has been verified against a full-wave EM simulator (HFSS). CNT bundles as TSVs can be modeled by an equivalent material approach with "complex effective conductivity." Using the geometrical parameters from the ITRS, we have shown that SWCNTs (all metallic) have a lower high-frequency resistance than other materials. It has also been shown that among capacitance (C), conductance (G), resistance (R), and inductance (L), only R strongly depends on the

technology node, but the performance analysis has indicated that R has the least impact on performance, while C has the most. However, it is shown that inductance (L) plays an important role in determining V_{DD}/GND voltage variations and hence, would be important for noise analysis. The performance analysis has also indicated that the difference between TSVs for Cu, W, SWCNT, and MWCNT is not significant. However, the thermal analysis has indicated that CNT-based TSVs can offer advantages over Cu and W by providing better heat dissipation. Since, in addition, CNTs have better mechanical robustness and thermal stability, CNT bundles could be the material of choice for TSVs in emerging 3-D ICs.

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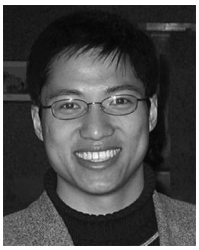

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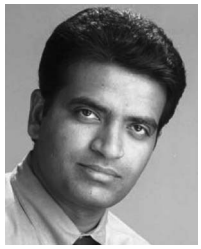

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