Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits

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***Abstract*—In this paper, novel n- and p-type tunnel field-effect transistors (T-FETs) based on heterostructure Si/intrinsic–SiGe channel layer are proposed, which exhibit very small subthreshold swings, as well as low threshold voltages. The design parameters for improvement of the characteristics of the devices are studied and optimized based on the theoretical principles and simulation results. The proposed devices are designed to have extremely low OFF currents on the order of 1 fA/μm and engineered to exhibit substantially higher ON currents compared with previously reported T-FET devices. Subthreshold swings as low as 15 mV/dec and threshold voltages as low as 0.13 V are achieved in these devices. Moreover, the T-FETs are designed to exhibit input and output characteristics compatible with CMOS-type digital-circuit applications. Using the proposed n- and p-type devices, the implementation of an inverter circuit based on T-FETs is reported. The performance of the T-FET-based inverter is compared with the 65-nm low-power CMOS-based inverter, and a gain of $\sim 10^4$ is achieved in static power consumption for the T-FET-based inverter with smaller gate delay.**

***Index Terms*—Band-to-band (B2B) tunneling, energy-efficient device, low power (LP), sub-kT/q device, subthreshold swing, tunnel field-effect transistor (T-FET).**

I. Introduction

STEEP subthreshold-slope or small subthreshold-swing devices are of great interest and significance in light of increasing subthreshold leakage current, which constitutes a major concern not only for power dissipation of digital ICs but also for their energy efficiency. As MOSFETs are scaled below 45 nm, the phenomenon of subthreshold leakage becomes more significant because of short-channel effects and increasing parameter variations [1], as well as strong coupling between temperature and subthreshold leakage current [2].

The leakage power is strongly influenced by the subthreshold swing of a device defined as $S = (\mathrm{d}\log I_{\mathrm{DS}}/\mathrm{d}V_{\mathrm{GS}})^{-1}$, where I_{DS} is the drain-to-source current under an applied gate-to-source voltage V_{GS}. The S indicates the minimum amount of gate-voltage reduction necessary to lower the subthreshold current by a factor of ten. Fig. 1 shows the minimum reported values of S for various classical and nonclassical CMOS, as well as nonsilicon solid-state devices [3]–[7]. It can be observed that all of the CMOS-based transistors [Bulk, FinFET, and fully-depleted silicon-on-insulator (FDSOI)] have S values $\geq$ 60 mV/dec $(= 2.3$ kT/q$)$ at room temperature, while the nanowire field-effect transistor (NWFET) [4], the carbon-nanotube-based tunnel field-effect transistor (T-CNFET) [6], [7], and the impact-ionization MOS-based transistor (IMOS) [5] have lower values of S (sub-kT/q). However, these devices suffer from difficulties in chip implementation, in terms of fabrication process or high-voltage requirements for operation. Among the new generations of sub-kT/q transistors, T-FET is a promising device due to its low OFF current [8]–[22] and integrability with CMOS process. It has been shown that T-FETs exhibit subthreshold swing smaller than 60 mV/dec [8]–[22]. Moreover, it has been shown that T-FETs can be scaled down to 20 nm in channel length, without much degradation of the subthreshold slope, I_{ON} and I_{OFF} [7], [12], [14]. However, T-FETs have lower ON currents and higher threshold voltages compared with MOSFETs. Although different T-FET structures have been reported in the literature [9], [10], [19], and a vertical n-type T-FET has been proposed in [12] and [16] to improve I_{ON} and S, and an n-type double-gate T-FET using high-k material is proposed in [13] to improve performance, the ON currents reported in these works are well below that of CMOS, or they exhibit threshold voltages higher than 0.4 V. Moreover, as discussed in Section III-C, the reported p-type T-FETs usually require gate voltages larger than the power-supply voltage to operate [7], [15], [17], [21], which makes them difficult to be integrated in digital circuits. Circuit implementation of the

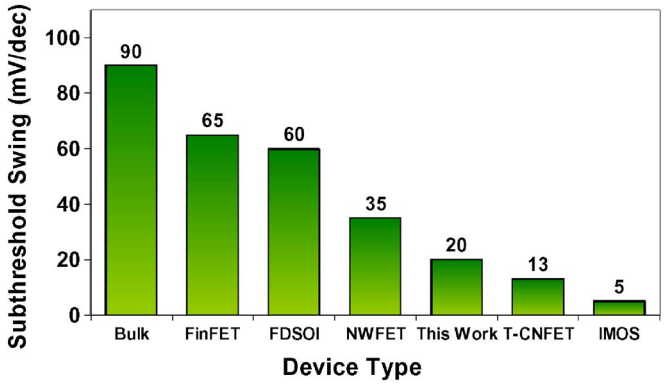

Fig. 1. Subthreshold swings (S) reported for various CMOS and emerging solid-state devices. CMOS devices show $S \geq 60$ mV/dec. The proposed T-FETs, T-CNFET, and IMOS devices exhibit the smallest values of S.

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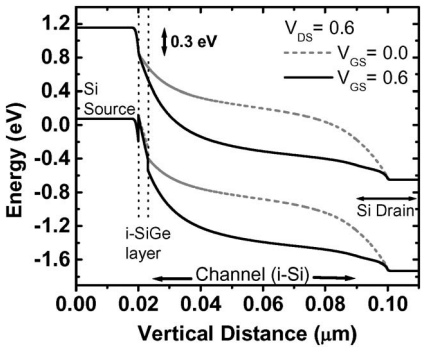

Fig. 2. Band profile for the proposed n-T-FET for different gate voltages. By applying sufficient gate voltage, current flows due to quantum tunneling of carriers. The intrinsic SiGe layer leads to improved S and $I_{\rm ON}$. By taking advantage of the small bandgap of SiGe, a lower gate voltage is required to bend the bands compared with the Silicon-based devices. Intrinsic doping of SiGe layer allows bending of the bands in this layer, resulting in higher ON current.

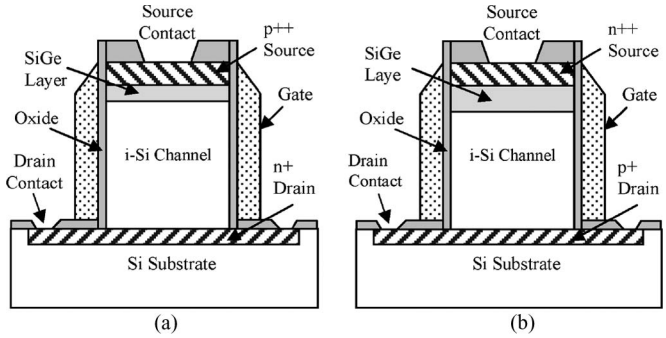

Fig. 3. Cross-sectional view of (a) n-type and (b) p-type vertical T-FET structures. The T-FETs are cylindrical gate-all-around structures. Source is heavily doped p/n type to 10^{20} cm^{-3} for n-T-FET/p-T-FET. Drain profile consists of a 20-nm doped region (5×10^{18} cm^{-3}) n/p type for n-T-FET/p-T-FET. The channel is intrinsic. $L_{\rm ch} = 70$ nm, $L_{\rm SiGe} = 3$ nm (for n-T-FET) and 12 nm (for p-T-FET). The Ge mole fraction for $Si_{1-x}Ge_x$ layer is 0.5 for n-T-FET and 0.3 for p-T-FET.

T-FETs has been of interest to some researchers. In [20], the circuit applications of Ge-based T-FETs are presented; however, due to low bandgap of germanium, the power-supply voltage is limited to 0.5 V, which leads to high delay.

In this paper, novel n- and p-type T-FETs based on heterostructure Si/intrinsic–SiGe channel layer are proposed to overcome the above mentioned limitations by studying the role of various design parameters for performance improvement of the devices using theoretical principles and simulation results. The proposed structures exhibit higher ON currents compared with previously reported T-FETs, S values as low as 15 mV/dec, and threshold voltages as low as 130 mV at ultralow $I_{\rm OFF}$. The proposed devices are also integrable in CMOS process and digital circuits. Using these T-FETs, an inverter circuit is implemented, and its transfer characteristics are studied. The performance of a LP 65-nm CMOS-based inverter (extracted from ITRS [23]) is compared with the T-FET-based inverter at the same supply voltage. In spite of having longer (65 nm) channel lengths, the T-FET devices proposed in this paper show significantly better characteristics compared with LP CMOS devices (65 nm). The T-FET-based inverter presented here provides more than $10^4\times$ savings in static power and exhibits smaller propagation delay compared with the CMOS-based inverter.

II. Device Structure and Working Principle

Interband tunneling was first observed in 1957 by Esaki [24] while studying narrow forward-biased p–n junctions called tunnel diode. This device has been used in LP microwave applications such as local oscillators for communication and high-speed sampling. A reverse-biased tunnel diode (Zener diode) can be used as a transistor by using a gate contact to control the band bending in the channel region [25].

Fig. 2 shows the band structure for the proposed p-i-n-based T-FET [Fig. 3(a)] along the channel. For $V_{\rm GS} = 0$, the tunneling barrier is large, and the device is in OFF state. Applying a positive gate voltage pushes the energy bands down and reduces the tunneling barrier. Due to reduced energy barrier, the carriers can tunnel from the valence band in the source to the conduction band in the channel, and the tunneling current will increase. The current is proportional to the electron/hole transmission probability $T(E)$ calculated through the Wentzel–Kramers–Brillouin (WKB) method, given by the first expression in (1) [26], [27]. For a planar T-FET device, $T(E)$ is given by the second expression in (1) [7]

$$T(E) \approx \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3|e|h(\Delta\phi + E_g)}\right) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|h(\Delta\phi + E_g)}\sqrt{\frac{\varepsilon_{\rm Si}}{\varepsilon_{\rm ox}}t_{\rm ox}t_{\rm Si}}\right) \quad (1)$$

where m^* is the carrier effective mass, e is the electron charge, E_g is the bandgap, $\Delta\phi$ is the energy range over which tunneling can happen (controlled by $V_{\rm GS}$), Λ is the spatial extent of the transition at the source–channel interface, $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm Si}$ are the dielectric constants of oxide and silicon, respectively, and $t_{\rm ox}$ and $t_{\rm Si}$ are the gate oxide and the silicon-layer thickness, respectively.

According to (1), the tunneling current increases by increasing the electric field along the channel (proportional to $(\Delta\phi + E_g)/\Lambda$). One way of increasing the electric field is to decrease the gate-oxide thickness or increase the dielectric constant. Another approach to improve the performance of the device is to decrease the bandgap in the channel, [from (1)]. The silicon-based channel can be completely replaced by a low-bandgap material such as SiGe or Ge [17], [20], or a thin layer of SiGe material can be used between the source and the channel [12]. Replacing the channel with SiGe or Ge increases the OFF current of the transistor because of the small bandgap of these materials, which significantly reduces the tunneling barrier even at low applied gate voltages. In this paper, a thin layer of low-doped $Si_{1-x}Ge_x$ is used between the source and the channel.

The structures of the n- and p-type silicon-based vertical T-FETs are shown in Fig. 3. The n-type device [Fig. 3(a)] consists of a degenerately doped (1×10^{20} cm^{-3}) p^{++} silicon-based source on top, a 3-nm intrinsic $Si_{1-x}Ge_x$ layer, 70-nm intrinsic silicon channel, and an n$^+$ (5×10^{18} cm^{-3}) drain

region. The low-doped drain reduces the OFF current [15]. The gate is an all-around structure made of n^+ polysilicon. The p-type device [Fig. 3(b)] consists of n^{++} silicon-based source on top, 12-nm intrinsic SiGe layer, 60-nm intrinsic silicon layer, and a $p^+(5 \times 10^{18}\ \mathrm{cm}^{-3})$ drain region. The gate is an all-around structure made of p^+ polysilicon. Oxide material is SiO_2, and its thickness is 1.5 nm for both devices. The device diameter is 80 nm. The critical (upper limit) thickness of the embedded SiGe layer decreases as the germanium mole fraction is increased [28], due to the stress induced by this layer. Hence, the Ge mole fraction is chosen to be 0.5 for the n-T-FET and 0.3 for the p-T-FET. In reality, it is not possible to have abrupt doping profiles at the source–channel and drain–channel junctions. Thus, a gradual doping profile is considered at the junctions and a uniform doping of $1 \times 10^{16}\ \mathrm{cm}^{-3}$ is used for the channel. Since the carrier tunneling happens near the source junction, the doping profile over the source junction is more important compared with that of the drain junction. In this paper, a junction abruptness of 1.8 nm/dec is used for the source junction. The junction abruptness near the drain is 5 nm/dec. The device can be fabricated by molecular-beam-epitaxy process [12], [18] or CVD process [29], [30].

Two-dimensional simulations were carried out using the 2-D device simulator MEDICI [31]. MEDICI uses Kane's model [35] to calculate the band-to-band (B2B) tunneling probability. The threshold voltage (V_{th}) of tunnel FETs cannot be extracted using the standard MOSFET techniques. Thus, V_{th} is calculated by a constant-current method at $I_D = 10^{-7}\ \mathrm{A}/\mu\mathrm{m}$. To calculate the subthreshold swing of the devices, the average current between the gate voltage at which I_D begins to increase and the threshold voltage of the device is considered [34].

III. Results and Discussion

A. n-Type T-FET With SiO_2 Gate Oxide

B2B tunneling is strongly dependent on the tunneling-barrier height and width that is controlled by the gate voltage. Fig. 2 shows the simulated conduction band and valence band for the proposed n-type T-FET under two values of gate bias, close to the $\mathrm{Si}-\mathrm{SiO_2}$ interface. For low V_{GS}, the tunneling width is bigger, but it decreases as V_{GS} is increased.

The tunneling probability is high near the source region. The bandgap E_g at the tunneling junction determines the tunneling-barrier height. The SiGe layer has a smaller bandgap compared with silicon. Hence, the barrier height can be engineered at the junction by changing the mole fraction of Ge (x). The bandgap decreases as x is increased [32], and considering the exponential dependence of the B2B tunneling probability on E_g in (1), higher tunneling current can be achieved by using the SiGe layer.

The electron affinity levels of Si and SiGe materials are such that almost all of the bandgap discontinuity occurs in the valence band. Thus, as shown in Fig. 2, the conduction band at the source–SiGe interface bends down smoothly by 0.3 eV. An applied gate voltage bends the bands further down in energy to increase the tunneling probability, and, since the conduction band is already bent down by 0.3 eV, the required gate voltage to reach a certain tunneling current is thereby reduced in comparison with a device that is completely based on silicon.

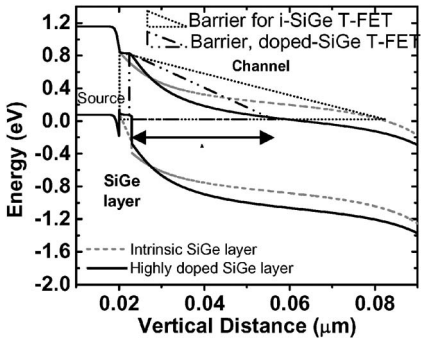

Fig. 4. Approximating the B2B tunneling barrier with a triangular potential barrier for i-SiGe-based T-FET and doped-SiGe-based T-FET at $V_{\mathrm{DS}} = 0.6$ V and $V_{\mathrm{GS}} = 0.0$ V (OFF state for both devices). The i-SiGe-based device has a larger tunneling barrier and shows lower OFF current compared with the highly doped-SiGe-based T-FET. At $V_{\mathrm{GS}} = 0.6$, the i-SiGe-based device has higher ON current due to band bending in the SiGe layer.

Other than using an intrinsic SiGe layer, another approach in designing the T-FET is to highly dope the SiGe layer as discussed in [12] and [16]. Fig. 4 shows the band diagram for such a device (solid line) as well as the band diagram for the proposed device (dashed line). Degenerate doping of the SiGe layer on the order of $1 \times 10^{20}\ \mathrm{cm}^{-3}$ (heavily doped δp^+ layer) raises the valence band at the tunneling junction, which reduces the tunneling barrier. While this effect increases the ON current of the device, it also increases the tunneling probability at $V_{\mathrm{GS}} = 0$; thus, the OFF current also increases. The increased I_{OFF} limits the power-consumption/energy-efficiency of the device.

Approximating the B2B barrier with a triangular potential, as indicated by the triangles in Fig. 4, the tunneling probability is calculated analytically using the WKB approximation [refer to (1)]. It can be observed that the spatial extent of the transition Λ at the source–channel interface is larger for the intrinsic SiGe-based device (i-SiGe) at $V_{\mathrm{GS}} = 0$. Thus, the barrier width is larger, and the tunneling current in the OFF state will be lower for the i-SiGe-based T-FET compared with the T-FET with highly doped SiGe layer. Simulation results also indicate that for the same applied V_{GS}, the proposed i-SiGe-based T-FET has significantly higher ON current compared with the T-FET with highly doped SiGe layer. This is because of the fact that under high V_{GS}, bands can bend significantly in the i-SiGe layer, while the bands remain relatively flat in the heavily doped SiGe layer. In a fabricated device, the vertical distribution of dopants can increase the doping level of the SiGe layer. This effect has been considered in simulations, and it was observed that increasing the SiGe layer's doping up to $10^{18}\ \mathrm{cm}^{-3}$ has a negligible effect on the overall performance of the device.

Fig. 5 shows the simulated transfer characteristics of the n-T-FET device (both with SiO_2 and HfO_2), and the effect of germanium mole fraction on the I_{DS}–V_{GS} curve. For low values of V_{GS}, the tunneling current is very small, and the reverse-biased p-i-n diode characteristics are dominant, resulting in small I_{DS}. As V_{GS} is increased, the bands bend, and the tunneling probability increases, allowing more current to flow.

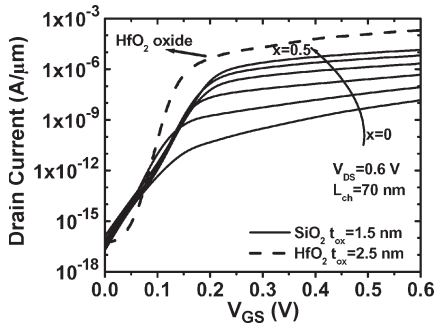

Fig. 5. Transfer characteristics of the vertical n-T-FET, for (dashed line) HfO_2 at $x = 0.5$ and for (solid line) SiO_2 for $x = 0.0$ to $x = 0.5$; x is mole fraction of Ge in SiGe layer. Increasing x results in higher $I_{\rm ON}$ and lower S, with small effect on $I_{\rm OFF}$.

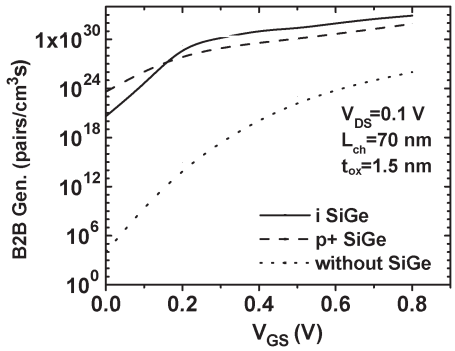

Fig. 6. B2B generation rate $(G_{\rm B2B})$ of n-T-FET for 1) intrinsic SiGe layer, 2) heavily doped SiGe layer [12] and 3) without SiGe layer. The proposed device with undoped SiGe layer shows higher $G_{\rm B2B}$ at high $V_{\rm GS}$ and low $G_{\rm B2B}$ at low $V_{\rm GS}$, resulting in better ON current and lower OFF current.

It can be observed from Fig. 5 that increasing the Ge mole fraction x from 0 to 0.5 improves the device characteristics, in terms of the ON current and threshold voltage. By increasing x, the SiGe layer bandgap becomes smaller [32], the tunneling-barrier height decreases, and the $I_{\rm ON}$ increases. The effect of Ge mole fraction on $I_{\rm OFF}$ is negligible because the tunneling current of the device in the OFF state is very small compared with the reverse-bias current of the p-i-n diode. The threshold voltage of the device with $x = 0.5$ is 0.2 V, which is measured at the constant current of 1×10^{-7} A/μm. Considering the low OFF current of the tunnel FET with such a low threshold voltage, the proposed T-FET can be used to design ultralow power circuits. The S for the SiO_2-based device is extracted as 20 mV/dec from Fig. 5. As the threshold voltage of the device increases by reducing the mole fraction, the average subthreshold-swing increases.

The outstanding characteristics of the device were also studied by considering the B2B generation rate at the source–channel junction (Fig. 6). Kane's model [35] for B2B generation rate $(G_{\rm B2B})$ is used in MEDICI device simulator to calculate the tunneling current and is given by [31]

$$G_{\rm B2B} = A_{\rm B2B} \frac{E^{C_{\rm B2B}}}{E_g^{1/2}} \exp\left(-B_{\rm B2B} \frac{E_g^{3/2}}{E}\right) \qquad (2)$$

where the parameters $A_{\rm B2B}$, $B_{\rm B2B}$, and $C_{\rm B2B}$ are user adjustable. E is the magnitude of the electric field, and E_g is the energy bandgap. The default values for these parameters are: $A_{\rm B2B} = 3.5 \times 10^{21}$ $({\rm eV}^{1/2}/{\rm cm} \cdot {\rm s} \cdot {\rm V}^2)$, $B_{\rm B2B} = 22.5 \times 10^6$ $({\rm V/cm} \cdot ({\rm eV})^{3/2})$, and $C_{\rm B2B} = 2.0$, for silicon. The values of $A_{\rm B2B}$ and $B_{\rm B2B}$ were modified to account for the decrease in reduced mass in the SiGe layer.

According to Fig. 6, at high values of $V_{\rm GS}$, the B2B generation rate is several orders of magnitude larger for SiGe-based devices. For the proposed device (i-SiGe), it is about two orders of magnitude larger compared with previously reported device [12], and, therefore, the proposed device shows higher ON current. At low values of $V_{\rm GS}$, the $G_{\rm B2B}$ is lower for the proposed device, which reduces the $I_{\rm OFF}$. Thus, the small bandgap of SiGe and the band bending in this layer have led to the improved B2B generation rate of the device resulting in improved $I_{\rm ON}$, S, and lower $V_{\rm th}$.

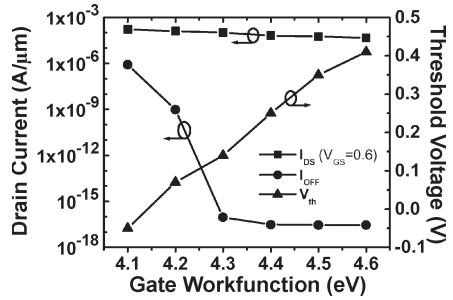

Fig. 7. Effect of gate workfunction on the performance of high-k gate-oxide-based n-T-FET. $I_{\rm OFF}$ is measured at $V_{\rm GS} = 0$ V, and $I_{\rm DS}$ is measured at $V_{\rm GS} = 0.6$ V and $V_{\rm DS} = 0.6$.

B. n-Type T-FET With High-k Gate Oxide

According to (1), the tunneling probability increases by using a gate-oxide material with higher dielectric constant. In this section the vertical i-SiGe-based T-FET using a high-k gate-oxide material, such as HfO_2 with a dielectric constant of 25 and oxide thickness of 2.5 nm, is studied. The structure of the device is the same as shown in Fig. 3(a), but the oxide material and the oxide thickness have been changed. The simulated input characteristics for the n-type T-FET with high-k material with $x = 0.5$ is shown in Fig. 5 and compared with the device with SiO_2 gate oxide. The high-k material offers better $I_{\rm ON}$ and subthreshold swing because of the improved coupling between the gate and the channel [33]. This is in agreement with the results in [13] where a double-gate silicon-based device with high-k material is studied. The band profile for this device is similar to the band profile of the SiO_2-based n-T-FET shown in Fig. 2 (with flatter bands in the i-channel region due to improved electrostatic control of the gate over channel potential), and is not shown here to avoid repetition.

The potential inside the channel at equilibrium and under zero bias is determined by the built-in voltage of the p-i-n structure, and the flatband voltage. The flatband voltage $V_{\rm FB}$ is defined as the difference between the gate workfunction and the channel workfunction at equilibrium. Thus, the gate workfunction has a direct effect on the flatband voltage and band bending in the channel. Fig. 7 shows the effect of gate workfunction on the performance of the device: the lower the gate workfunction,

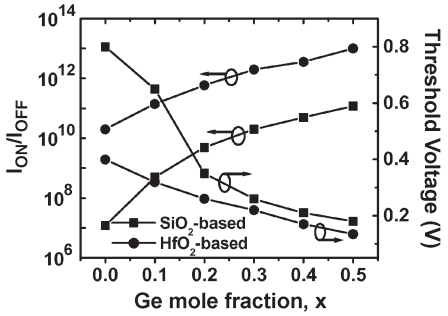

Fig. 8. (Left y-axis) $I_{\rm ON}/I_{\rm OFF}$ ratio and (right y-axis) threshold voltage for high-k-based and SiO_2-based n-T-FET devices as a function of Ge mole fraction x. A higher value of x improves the performance of both devices.

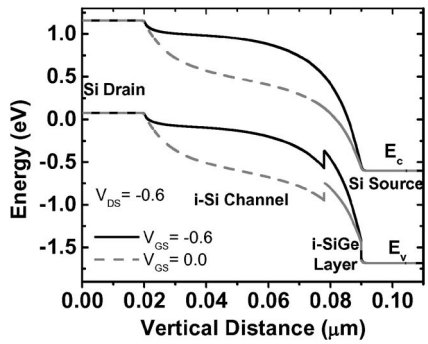

Fig. 9. Band profile of SiO_2-based p-T-FET for different values of gate voltage. Using a 10-nm SiGe layer and workfunction engineering, the bands are bent at $V_{\rm GS} = -0.6$, allowing tunneling current to flow. By increasing $V_{\rm GS}$, the current will decrease.

the higher the downward band bending in the channel near the source–channel junction. This leads to an increase in the $I_{\rm OFF}$ of the device. At high values of $V_{\rm GS}$ (ON state), $I_{\rm DS}$ is a weak function of $V_{\rm GS}$ and band bending, and the device shows similar characteristics as a saturated MOSFET. However, the gate workfunction controls the threshold voltage of the device. By choosing a high value for workfunction, the bands are pushed upward in energy along the channel because of the coupling between the gate and the channel, thereby reducing the tunneling probability. Hence, in engineering the gate workfunction, there is a tradeoff between the OFF current and threshold voltage of the device. In this paper, the gate workfunction is chosen to be 4.3 eV, to get both low $I_{\rm OFF}$ and low $V_{\rm th}$. The simulation results show an ON current of 120 μA/μm for SiO_2-based n-TFET and 1300 μA/μm for high-k-based n-T-FET at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.0$ V. The high-k-based n-T-FET exhibits a threshold voltage of 0.13 V and subthreshold swing of 15 mV/dec (Fig. 5).

Furthermore, the effect of Ge mole fraction x on the performance of the n-T-FET has been investigated. It was shown in Fig. 5 that a higher value of x improves the $I_{\rm ON}$, S, and $V_{\rm th}$. In Fig. 8, the effect of x on the $I_{\rm ON}/I_{\rm OFF}$ ratio and the threshold voltage of the SiO_2-based and high-k-based n-T-FET is shown. Increasing the value of x from 0 to 0.3 decreases the threshold voltage of both devices. Further increase in x from 0.3 to 0.5 does not decrease the threshold voltage significantly, but the higher the Ge mole fraction, the higher is the $I_{\rm ON}/I_{\rm OFF}$ ratio, which lends support to the use of SiGe layer with $x = 0.5$.

C. p-Type T-FET With SiO_2 Gate Oxide

p-type MOSFETs have been used in numerous applications in integrated circuits for decades. In fact, the digital design area was boosted by the introduction of the complementary design, based on the use of both n- and p-type transistors to implement logic gates. The low subthreshold swing and ultralow power behavior of T-FETs make them interesting devices for digital applications. Thus, introduction of appropriate p-type T-FETs is necessary to make the T-FET technology compatible with digital circuit design.

T-FETs exhibit ambipolar behavior [13], [15]. When a negative V_G is applied (while the n^{++} region is biased at positive voltage and the p^{++} region is grounded), the bands bend upward in the channel region, and the tunneling probability of carriers from drain to channel increases, which leads to increased current. This property of the T-FET is used to form p-type T-FETs [15], [17], [21]. The reported p-channel devices have used biasing scheme, which requires a higher potential difference than $V_{\rm DD}$ between source and gate for proper functioning of the devices, that is not practical in typical digital circuits. Therefore, a modification of the device characteristics is required to make it compatible with digital applications, as a negative V_G is not available in most digital circuits. To do so, a high-workfunction gate material must be used to shift the input characteristics of the device (I_D versus V_G) along the V_G axis, so that the device is in OFF state at $V_G = V_{\rm DD}$, and is in ON state at $V_G = 0$ V. According to the device simulations, a gate workfunction of 5.6 eV is required for a purely silicon-based T-FET to exhibit characteristics compatible with digital applications, which is not feasible.

To overcome the problems mentioned previously, the T-FET structure is modified, and a p-T-FET device is proposed, which shows input behavior similar to p-type MOSFETs. The proposed device structure is shown in Fig. 3(b) and has been described earlier in this paper. Since the tunneling probability is higher near the n^{++} region, the SiGe layer is grown near this region, which is called source. Fig. 9 shows the band profile of the device along the channel near the channel–oxide interface. The drain (p^+) is grounded, and the source (n^{++}) is connected to $V_{\rm DD}$. When the gate voltage is held at $V_{\rm DD}$ ($V_{\rm GS} = 0$), the tunneling barrier is large, and the drain current is negligible. By applying a zero voltage to the gate electrode ($V_{\rm GS} < 0$), the bands bend upward in energy, and the tunneling barrier becomes smaller, which increases the tunneling probability near the source junction. Because of the bandgap discontinuity at the source–channel junction between Si and SiGe, the valence band of the SiGe layer rises above the valence band of silicon; therefore, the small bandgap of SiGe further reduces the tunneling barrier and increases the B2B tunneling current. Without the SiGe layer, a higher value of $V_{\rm GS}$ (usually higher than $V_{\rm DD}$) is required to achieve high ON current.

Fig. 10 shows the threshold voltage and the $I_{\rm ON}/I_{\rm OFF}$ ratio for this p-T-FET as a function of the thickness of the SiGe layer. As can be seen in the figure, the $I_{\rm ON}/I_{\rm OFF}$ ratio has a maximum value when the thickness of the SiGe layer is 12 nm, and the threshold voltage drops as the thickness increases. The

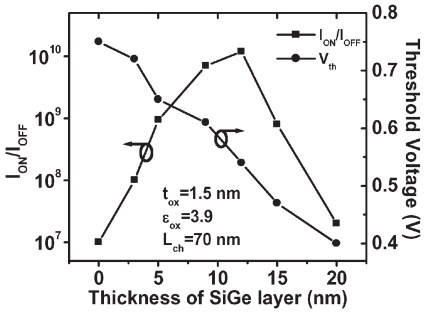

Fig. 10. $I_{\rm ON}/I_{\rm OFF}$ ratio and threshold voltage of SiO_2-based p-T-FET versus thickness of SiGe layer. The threshold voltage decreases as the thickness increases, but the $I_{\rm ON}/I_{\rm OFF}$ ratio reaches its maximum value with a SiGe layer of 12 nm width.

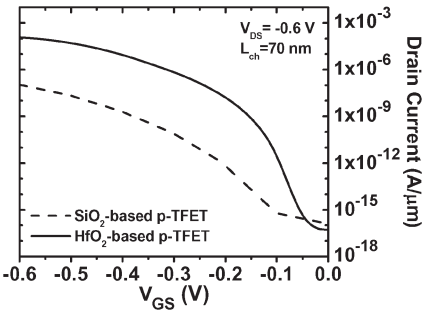

Fig. 11. Input transfer characteristics of vertical p-T-FET, using SiO_2 with $x = 0.3$ and HfO_2 with $x = 0.3$, The high-k material gives better $I_{\rm ON}$, S, and $V_{\rm th}$. Using high-k material, the magnitude of $V_{\rm th}$ is reduced from 0.54 to 0.22 V, and S is reduced from 50 to 22 mV/dec. Gate-oxide thickness is 1.5 nm for SiO_2 and 2.5 nm for HfO_2.

reason for such a behavior can be understood by studying the band diagram. Using a thin layer of SiGe, the required band bending to turn on the device cannot be achieved, and the $I_{\rm ON}$ will decrease and $V_{\rm th}$ will increase. Furthermore, because of its small bandgap, a thick SiGe layer results in higher band bending near the source–channel region and higher tunneling probability that increases the OFF current of the device and reduces the $I_{\rm ON}/I_{\rm OFF}$ ratio. Hence, the thickness of the SiGe layer is chosen to be 12 nm to get the best $I_{\rm ON}/I_{\rm OFF}$ with a reasonable threshold voltage of 0.54 V. The Ge mole fraction x is 0.3. A higher value of x improves the performance but is impractical due to reduced critical thickness of SiGe layer as x is increased [28]. To get lower threshold voltage, a higher value of SiGe layer thickness can be chosen at the cost of reduced $I_{\rm ON}/I_{\rm OFF}$ ratio. The data shown in Fig. 10 is measured from the simulations for the p-T-FET with p^+ polysilicon as the gate material.

The gate workfunction has a direct effect on the band bending inside the channel as discussed in Section III-B. Choosing a high value of workfunction for the gate material pushes the energy bands upward, while a lower workfunction pushes the bands downward. To increase the $I_{\rm DS}$, the bands must bend upward (near the source) as much as possible. Thus, the gate material is chosen to have a high workfunction, such as p^+ polysilicon.

The input characteristic for the optimized p-T-FET is shown in Fig. 11. The device has low OFF current, and the magnitude of the threshold voltage is 0.54 V. The subthreshold swing of the simulated device is 50 mV/dec. The input characteristics of the device are very similar to that of a p-type MOSFET. Therefore, the device can be combined with the n-T-FET for digital-circuit applications. The input characteristic of the p-T-FET with high-k material is also shown in the Fig. 11 and will be discussed in the next section.

D. p-Type T-FET With High-k Gate Oxide

Compared with the n-T-FET, the SiO_2-based p-T-FET shows lower ON current and higher subthreshold swing. In order to use n- and p-type T-FETs in complementary logic circuits, it is best for the devices to have similar characteristics, such as symmetric rise and fall times, which are dependent on the ON current and output/input capacitance of the device. One approach to have similar ON currents for n- and p-type devices is to use the vertical n-T-FET with smaller diameter to decrease the drive current, but, since the drive current of the n-T-FET is substantially higher than that of the p-T-FET (in the case of SiO_2-based devices), the sizing method is not practical. The other approach is to modify the band bending in the channel, which is possible, by improving the coupling between the gate and the channel using high-k gate oxide. As shown earlier in Section III-B, the high-k gate oxide improves the $I_{\rm ON}$ and S, and lowers the $V_{\rm th}$ of the n-T-FET. In this section, the high-k material HfO_2, with dielectric constant of 25, is used as the oxide layer for the p-T-FET. The device structure is the same as the one used for the SiO_2-based p-TFET, but the gate-oxide layer is replaced by high-k material. The oxide thickness is 2.5 nm, and the SiGe layer thickness is 3 nm with $x = 0.3$. The SiGe layer reduces the tunneling barrier at the source–channel junction. A higher thickness for SiGe layer increases the OFF current of the device, as shown earlier in Fig. 10, for the SiO_2-based p-T-FET. The band diagram for high-k-based p-T-FET is similar to the SiO_2-based p-type device in Fig. 9 (with flatter bands in the i-channel region due to improved electrostatic control of gate over channel potential).

Due to improved control over channel by the gate electrode, the high-k-based p-T-FET shows better performance compared with the SiO_2-based p-T-FET. The input characteristic of the high-k-based device is shown in Fig. 11 and is compared with that of the device with SiO_2-based gate oxide. The magnitude of the threshold voltage for this device is reduced to 0.22 V, compared with 0.54 V for the SiO_2-based device. Moreover, the subthreshold swing of the device shows a substantial improvement to 22 mV/dec, and the ON current of the device is 1100 μA/μm, measured at $V_{\rm DS} = -1.0$ V, and $V_{\rm GS} = -1.0$ V, and the drain current at $V_{\rm DS} = -0.6$ V, and $V_{\rm GS} = -0.6$ V is 100 μA/μm, which meets the technology requirement according to ITRS for the 45-nm LP node. The $I_{\rm OFF}$ is still very small and on the order of 10^{-15} A/μm.

IV. Circuit Implementation

Using the high-k-based n- and p-type T-FET devices (with $x = 0.5$ for n-T-FET, and $x = 0.3$ for p-T-FET), a T-FET-based inverter circuit is reported in this paper. The circuit is shown in Fig. 12. The n^{++} region (source) of the p-T-FET is connected to $V_{\rm DD}$, and the n^+ region (drain) of the n-T-FET is connected to $V_{\rm out}$. In this way both the n- and p-type devices are

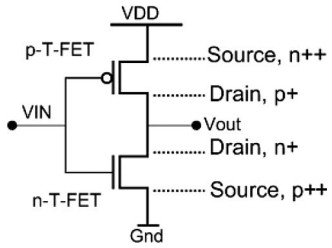

Fig. 12. Inverter-circuit schematic using T-FETs. Both T-FETs must be in reverse-biased region. Unlike MOSFETs, the T-FET device is not a symmetric device, and special care is needed when designing circuits to avoid forward-biased p-i-n structures. Tunneling happens near the source region for both T-FETs.

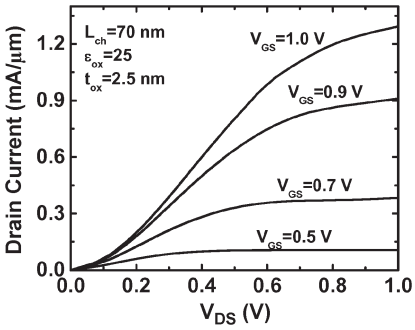

Fig. 13. Output transfer characteristics of vertical n-T-FET, using high-k gate oxide with $x = 0.5$. Like MOSFET, saturation behavior is observed.

configured in the circuit to work in the reverse-biased regime. The characteristics of the devices are modeled in HSPICE using behavioral elements. The intrinsic gate capacitances are extracted using MEDICI, while the extrinsic capacitances are estimated using simple analytical models. The n- and p-type devices are designed to exhibit similar input/output characteristics. Fig. 13 shows the output characteristics of the n-type T-FET device with high-k gate oxide. Similar to MOSFETs, the T-FET exhibits saturation behavior since the tunneling-barrier width becomes progressively less dependent on $V_{\rm DS}$ for high values of $V_{\rm DS}$. For $V_{\rm DS} < 0.2$ V, the drive current of the T-FET is strongly dependent on $V_{\rm DS}$, which will be more apparent on a log–linear scale.

In this section, the characteristics of the T-FET-based 1 : 1 inverter is compared with that of a 65-nm CMOS-based 2 : 1 inverter. For the CMOS model, the predictive technology model [36] for 65-nm LP technology node is used. For CMOS transistors, the $V_{\rm th}$ must be increased to achieve low OFF current. The increase in $V_{\rm th}$ results in low ON current ($\sim$400 μA/μm), which increases the delay of the circuits. On the other hand, because of its low S, the proposed T-FET devices exhibit low OFF current as well as high ON current. Therefore, the proposed T-FETs can be used in LP applications as well as low standby power (LSTP) applications with lower delay compared with LP and LSTP CMOS transistors.

The dc characteristic of the inverter is investigated and the voltage-transfer curve (VTC) for the inverter is shown in Fig. 14. The inverter has a gain of 12 V/V. An external load capacitance (C_L) is attached to the output of the inverter and the propagation delay (50% of input to 50% of output) and

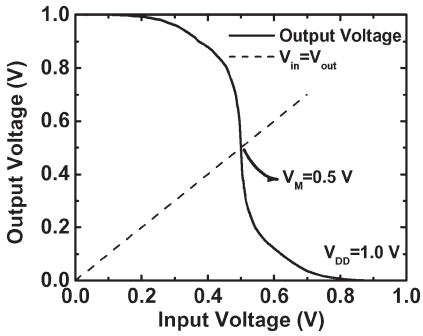

Fig. 14. VTC curve for the T-FET-based inverter. Gain is equal to 12 V/V in the transition region. By employing bandgap and workfunction engineering, both n- and p-type devices were designed to exhibit similar input/output characteristics.

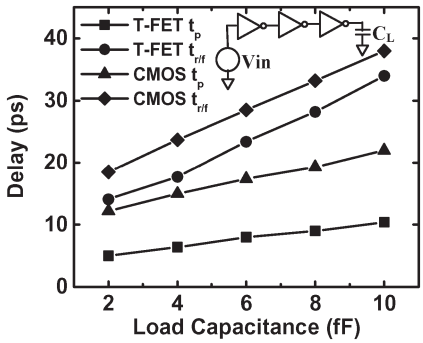

Fig. 15. Comparison of delay for LP CMOS and the proposed T-FET-based inverters. Propagation delay (t_p) and rise/fall time $(t_{r/f})$ for the inverter driving C_L are measured for different values of external load capacitance.

the rise/fall time (10% to 100% or 100% to 10% of output) of the CMOS-based and T-FET-based inverters for $C_L = 2$ to 10 fF are measured in HSPICE (Fig. 15). By choosing such large values for C_L, any possible error that could be introduced by the gate-capacitance ($C_{\rm gs}$ and $C_{\rm gd}$) extraction method and Kane's model (due to overestimation of current at low values of $V_{\rm DS}$ in MEDICI) is suppressed.[1] The width of the NMOS device is 1 μm, and the perimeters of the n- and p-type T-FET devices are 1 μm. Several T-FET devices are used in parallel to achieve the desired perimeter. Two inverter stages of the same size are employed before the main inverter (driving C_L) to reduce signal-feedthrough effect at the output of the main inverter. The measured delays are with respect to the input and output of the third inverter. The T-FET-based inverter shows more than 2$\times$ improvement in propagation delay (t_p) compared with the CMOS-based inverter, which is attributed to the T-FET's higher ON current and lower $V_{\rm th}$. The rise/fall time $(t_{r/f})$ of the T-FET-based inverter is slightly better than that of the CMOS inverter. In [37] it is argued that because of their low drive currents at low $V_{\rm DS}$ values, the T-FETs exhibit very large rise/fall times compared with

[1]The intrinsic output capacitance of the inverter $(C_{\rm int})$ depends on $C_{\rm gd}$ (gate–drain cap.). With the 1-μm perimeter for T-FET, the $C_{\rm gd}$ is very small compared with C_L, which is varied from 2 to 10 fF. The $C_{\rm gs}$ (gate–source capacitance), which is comparable with the lower limit of C_L, does not contribute to the delay directly. The only effect $C_{\rm gs}$ can have is on the rise/fall time of the input signal of the third inverter, which is negligible compared with the delay of the inverter because of C_L.

TABLE I
COMPARISON OF VARIOUS T-FET DEVICES REPORTED IN THE LITERATURE AND IN THIS PAPER. THE ITRS REQUIREMENT FOR 45-nm LSTP AND 32-nm LP MOSFET ARE ALSO SHOWN FOR COMPARISON

Reference	Channel length (nm)	Type	$\|V_{DS}\|$ (V)	$\|V_{GS}\|$ (V)	S* mV/dec	I_{ON}** μA/μm	I_{OFF} fA/μm	V_{th} (V)	Dielectric constant (ε)	Channel material	t_{ox} nm	Suitable for digital circuit implementation
[12], [16]	100	n	1.0	2.0	50	1000	10	0.94	3.9	Si+SiGe	2	No
[17]	70	p	0.7	4.5	>100	1	1000	>1	3.9	Si+SiGe	4.5	
[14]	100	n	1.0	1.5	~85	~10	<0.1	0.94	3.9	Si	3	-
[14]	100	n	1.0	1.5	52	~140	<0.1	0.6	25	Si	3	
[7]	25	p	.3	-	13	-	~1	0.33	-	CNT	-	No
[15]	1000	n	3	4	471	0.2	8000	3.5	3.9	Si	6	No
[15]	1000	p	3	4	106	4	8000	2.2	3.9	Si	6	
[19]	70	n	1	1	52.8	20	10^6	0.12	3.9	Si	2	-
[22]	53	n	1.2	1.2	35	800	~0.1	~0.4	25	Si	3	-
[23] LSTP MOSFET	45	-	1.1	1.1	>60	465	$3x10^4$	0.40	-	Si	1.9	Yes
[23] LP MOSFET	32	-	0.8	0.8	>60	563	$9x10^6$	0.32	-	Si	1.2	Yes
This work	70	n	1.0	1.0	20	120	0.01	0.20	3.9	Si+SiGe	1.5	Yes
This work	70	n	1.0	1.0	15	1300	0.1	0.13	25	Si+SiGe	2.5	
This work	70	p	1.0	1.0	50	6	0.1	0.55	3.9	Si+SiGe	1.5	
This work	70	p	1.0	1.0	21	1100	0.05	0.22	25	Si+SiGe	2.5	

* The average current between the gate voltage, at which I_D begins to increase, and the threshold voltage of the device is considered to calculate S.
** I_{ON} is measured at the given V_{DS} and V_{GS}.

those of CMOS devices. However, the CMOS model used and the device dimensions employed were not explicitly stated. In this paper, the measured $t_{p,\mathrm{T-FET}}/t_{p,\mathrm{CMOS}}$ is smaller than $t_{r/f,\mathrm{T-FET}}/t_{r/f,\mathrm{CMOS}}$, which suggests that t_p improvement is superior to $t_{r/f}$ improvement in T-FETs. However, the rise/fall time of the T-FET-based inverter is still lower than that of CMOS for the same output load. This is attributed to the low ON current of the LP CMOS transistors, which arises from increased V_{th} to achieve low OFF current. The static power consumption of the T-FET inverter shows $\sim 10^4\times$ improvement compared with the 65-nm LP CMOS inverter.

V. COMPARISON WITH T-FETS IN LITERATURE

Table I shows the characteristics of some of the recently reported T-FETs and the four T-FET devices proposed in this paper. The subthreshold swings of the devices proposed in this paper are significantly smaller than those of the previously reported devices based on Silicon or SiGe. To achieve smaller S values, carbon-nanotube-based T-FETs [7] can be used at the cost of significant process complexity. It can be observed that the proposed devices offer higher ON currents compared with other T-FET devices, even at lower V_{DS} and V_{GS} values. The ON current of the SiO_2-based p-T-FET is not as good as that of the other three proposed devices, and the use of p-T-FET with high-k material is preferred. All the T-FET devices shown in Table I, exhibit very low OFF current, which makes them strong candidates for LP and energy-efficient applications.

The threshold voltage is an important parameter in low-voltage design. The proposed devices exhibit substantially smaller threshold voltages compared with those of previously reported devices. The T-FET device reported in [19] exhibits lower threshold voltage, but the ON current and the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is smaller than that of the T-FETs proposed in this paper. Moreover, the proposed T-FET devices are compatible with digital-circuit design and can be used to build complementary logic gates. The table also provides the characteristics of the 32-nm (physical gate length) LP MOSFET and 45-nm (physical gate length) LSTP MOSFET design requirements from ITRS [23]. Compared with ITRS requirements, the proposed T-FETs exhibit lower S, I_{OFF}, and V_{th}, and the high-k-based T-FETs show higher ON currents.

VI. CONCLUSION

Gate all-around vertical n-type and p-type T-FETs based on heterostructure silicon/intrinsic-SiGe channel layer have been proposed, which are compatible with digital-circuit implementation. The T-FETs proposed are compared with the T-FETs reported in the literature. The proposed T-FETs show improved characteristics, including higher ON current, lower subthreshold swings (~15–20 mV/dec), and lower threshold voltages (0.13–0.22 V). The performance enhancements are achieved by optimizing various device parameters using theoretical principles and simulation results. The parameters include the doping profile of SiGe layer and drain, Ge mole fraction, SiGe layer thickness, gate workfunction, and oxide material.

Limitations of the reported p-type T-FETs in literature (in terms of circuit operation) are highlighted. The proposed p-type T-FETs were engineered to overcome such limitations. An inverter circuit based on these T-FETs with ultralow static power dissipation was designed. Compared with the 65-nm LP CMOS-technology node inverter, the T-FET-based inverter (with ~70-nm channel length) consumes $\sim 10^4$ times less static power, while the propagation delay is $2\times$ lower than that of the CMOS inverter for the same external load capacitance. The dc characteristics of the inverter and the improved behavior of the T-FETs suggest that, if designed properly, these devices can be strong alternatives to MOSFETs in ultralow power and energy-efficient digital-circuit applications.

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