University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #1

Due Date: Tuesday, May 23, at 4 pm in class (To be collected by Junkai Jiang)

Problem 1 Semiconductor Physics

a) Consider a cube of semiconductor crystal with length L on each side. Derive the density of electron states $D_{3D}(E)$. Similarly, derive the density of electron states for a 2-dimensional system $D_{2D}(E)$. Sketch the density of states for the 3D and 2D cases. Assume the electron effective mass is m_n.

b) In a silicon sample doped with 10^{17} cm^{-3} of phosphorus atoms, what fraction of the donors are not ionized. The donor level E_d is located at 45 meV below conduction band edge for phosphorus.

c) Use the Matthiessen's rule to calculate and plot the mobility vs. temperature $\mu(T)$ from 10 K to 500 K for Si doped with N_d = 10^{14}, 10^{16}, and 10^{18} donors cm^{-3}. Consider the mobility to be determined by impurity and phonon (lattice) scattering. Impurity scattering limited mobility can be described by

$$\mu_I = 3.29\times10^{15}\frac{\varepsilon_r^2 T^{3/2}}{N_d^+(m_n^*/m_0)^{1/2}[\ln(1+z)-\frac{z}{1+z}]}$$

where

$$z = 1.3\times10^3\varepsilon_r T^2(m_n^*/m_0)(N_d^+)^{-1}$$

Assume that the ionized impurity concentration N_d^+ is equal to N_d at all temperatures.

The conductivity effective mass m_n^* for Si is $0.26m_0$. Acoustic phonon (lattice) scattering limited mobility can be described by

$$\mu_{AC} = 1.18\times10^{-5}c_1(m_n^*/m_0)^{-5/2}T^{-3/2}(E_{AC})^{-2}$$

where the stiffness (c_1) is given by

$$c_1 = 1.9\times10^{12}\,dyne-cm^{-2} \text{ for Si}$$

and the conduction band acoustic deformation potential (E_{AC}) is

$$E_{AC} = 9.5eV \text{ for Si.}$$

Problem 2 MOS Capacitor CV

The MOS capacitor theory was covered in detail in the lectures (for p-type body). Using the lecture notes, repeat all derivations for an n-type body. All other parameters can be assumed to be same as those used for the p-type body. You may assume E_F-E_C = 0.4 eV

Draw the band diagrams and derive expressions for the following conditions:

a) Flat-band condition.

b) Surface-accumulation condition.

c) Surface-depletion condition.

d) Threshold condition and threshold voltage.

e) Strong-inversion (beyond V_T).

f) Using the expressions derived above in (a)-(e), plot the C-V characteristics of such MOS capacitor for both low and high frequency conditions.

Problem 3 MOSFET Scaling Issues

a) Based on your understanding of the so-called short-channel effect, what kind of electric field distribution inside the device is desirable to minimize this effect? Hint: make connection with DIBL.

b) Sketch the curve of carrier velocity vs. lateral electric field for a device in which velocity saturation occurs and briefly describe the cause of velocity saturation.

c) Analyze how velocity saturation affects the voltage-transfer-characteristics (VTC) of a balanced CMOS inverter.

d) In short channel MOSFETs, retrograded doping profile is usually adopted to suppress the punch-through effect. Please refer to the paper below to get familiar with such devices. Try to derive the expression of SS for these devices in the long-channel case. You can assume that the doping profile is abrupt at the junction between the lightly and highly doped layers. (Reference: Indranil De et al., "Impact of Super-Steep-Retrograde Channel Doping Profiles on the Performance of Scaled Devices," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, Aug. 1999.)

Problem 4 MOSFET Electrostatics

Read the paper on MOSFET scaling (R. H. Yan et al., "Scaling the Si MOSFET: From Bulk to SOI to Bulk," IEEE Transactions on Electron Devices, vol. 39, no. 7, pp. 499-502, 1992.). Derive the expressions for the Natural Length (λ) for the following devices:

a) Planar Bulk MOSFETs (with and without high-k dielectric)

b) Ultra-thin Body (UTB) SOI MOSFETs (partially depleted and fully depleted)

c) Double-gate FETs: (FinFET) and Tri-gate FET

d) Gate-all-around FET (or a nanowire FET)

Problem 5 Tunneling FETs

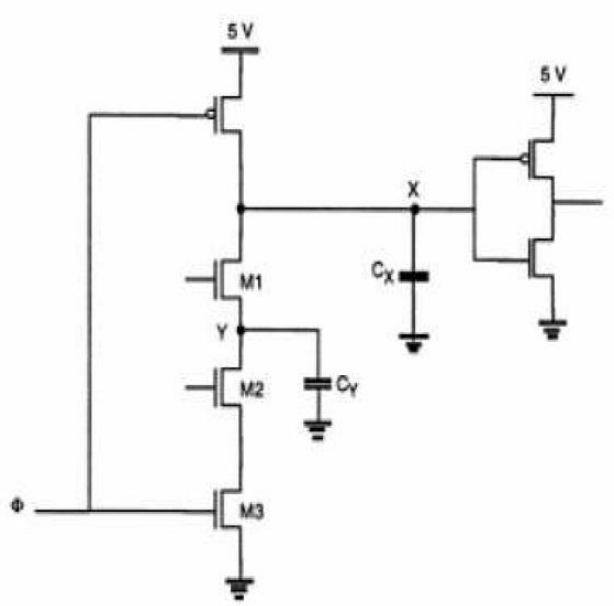
Please review lecture 6, slide 12 showing the slow V_{ds} turn-on.

a) Why the I_D-V_D is not linear at low V_D regime? Is this an intrinsic or extrinsic property? Is there any possibility to eliminate it? If tunnel FETs are used to design a 1T-DRAM, what effect could be expected?

b) Analyze the enhanced Miller effect in a tunnel FET based inverter with load capacitance, reproduce the figure (showing Miller effect) by SPICE simulation. (hint: you can use MOSFETs instead of tunne FETs in the simulation, and artificially change the capacitance).

Problem 6 CMOS Logic

Consider the CMOS logic circuit in the right figure, which is a simple Domino logic circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the Domino circuit.



(a) Explain how the voltage level at node X, after it is pre-charged to 5 V, can be affected during "evaluate" by the charge sharing between node X and node Y. Express the final voltage at node X in terms of the initial voltage at node Y, when the charge sharing is completed following the full pre-charge operation. During pre-charge, the gate terminal of the transistor M2 is fixed at 0 V.

(b) Determine the ratio between device transconductance parameters, kp and kn, of the inverter to prevent any logic error due to charge sharing between nodes X and Y under all circumstances. Assume that the magnitudes of threshold voltages in the inverter are equal to 1.0 V.