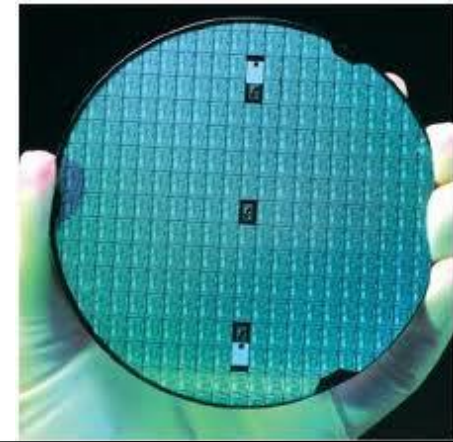
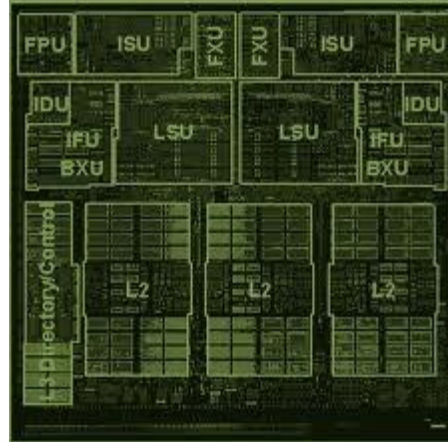
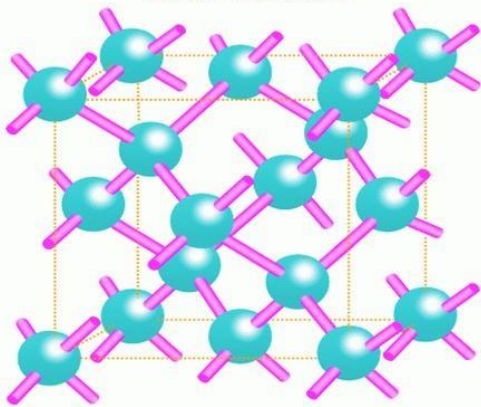


Structure of silicon crystal



ECE 225

Lecture 10

On-chip Inductance Effects

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara

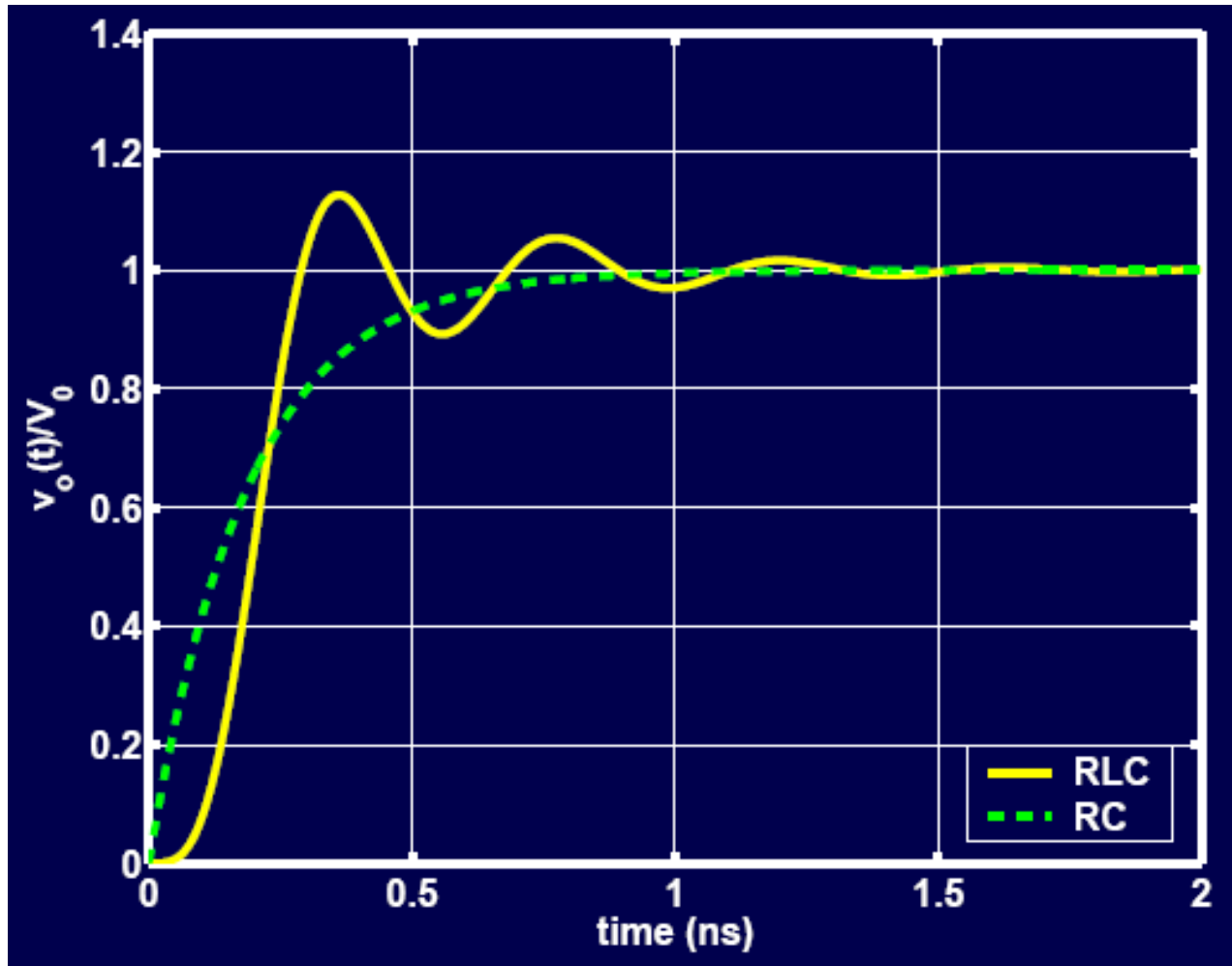
On-Chip Inductance Effects

K. Banerjee and A. Mehrotra, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 8, pp. 904-915, August 2002.

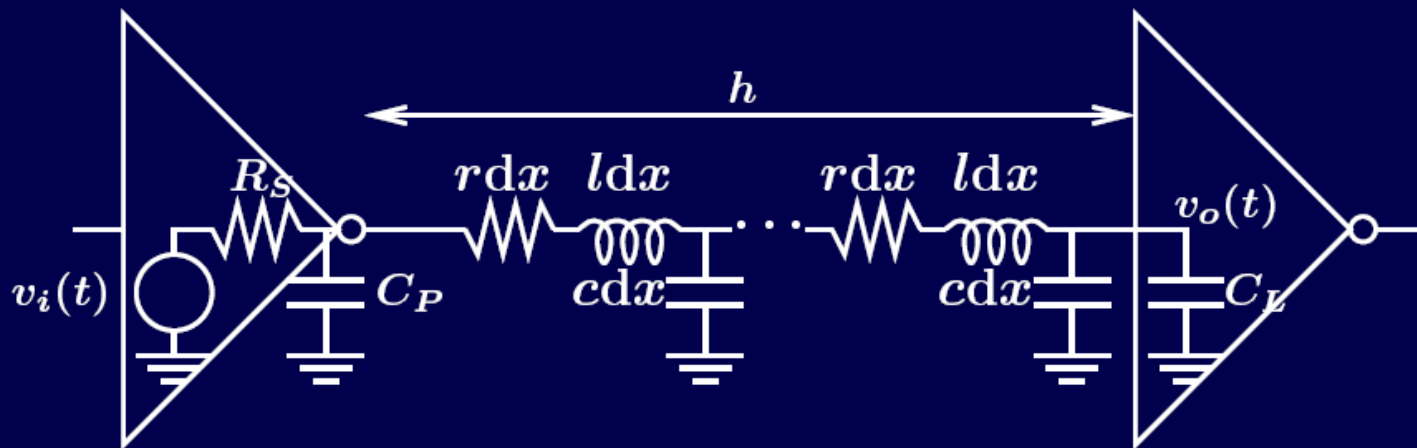
On-Chip Inductance Effects

- *Increasing clock speeds and decreasing rise times cause inductive effects*
- *Low resistance wires more susceptible to inductive effects*
 - *Global wires that are usually wide*
 - *introduction of Cu: lower resistivity*
- *Line inductance depends on current return path*
 - *strongly dependent on circuit topology*
 - *difficult to extract accurately*
 - *large variations*

Step Response of an RLC Line



Time-Domain Response of RLC Segment



$$H(s) = \frac{1}{[1 + sR_S(C_P + C_L)] \cosh(\theta) + \left[\frac{R_S}{Z_0} + sC_L Z_0 + s^2 R_S C_P C_L Z_0 \right] \sinh(\theta)}$$

$$\approx \frac{1}{1 + sb_1 + s^2 b_2 + s^3 b_3 + s^4 b_4}$$

$$Z_0 = \sqrt{\frac{r + sl}{sc}} \quad \theta = \sqrt{(r + sl)sc}h$$

Critical Inductance

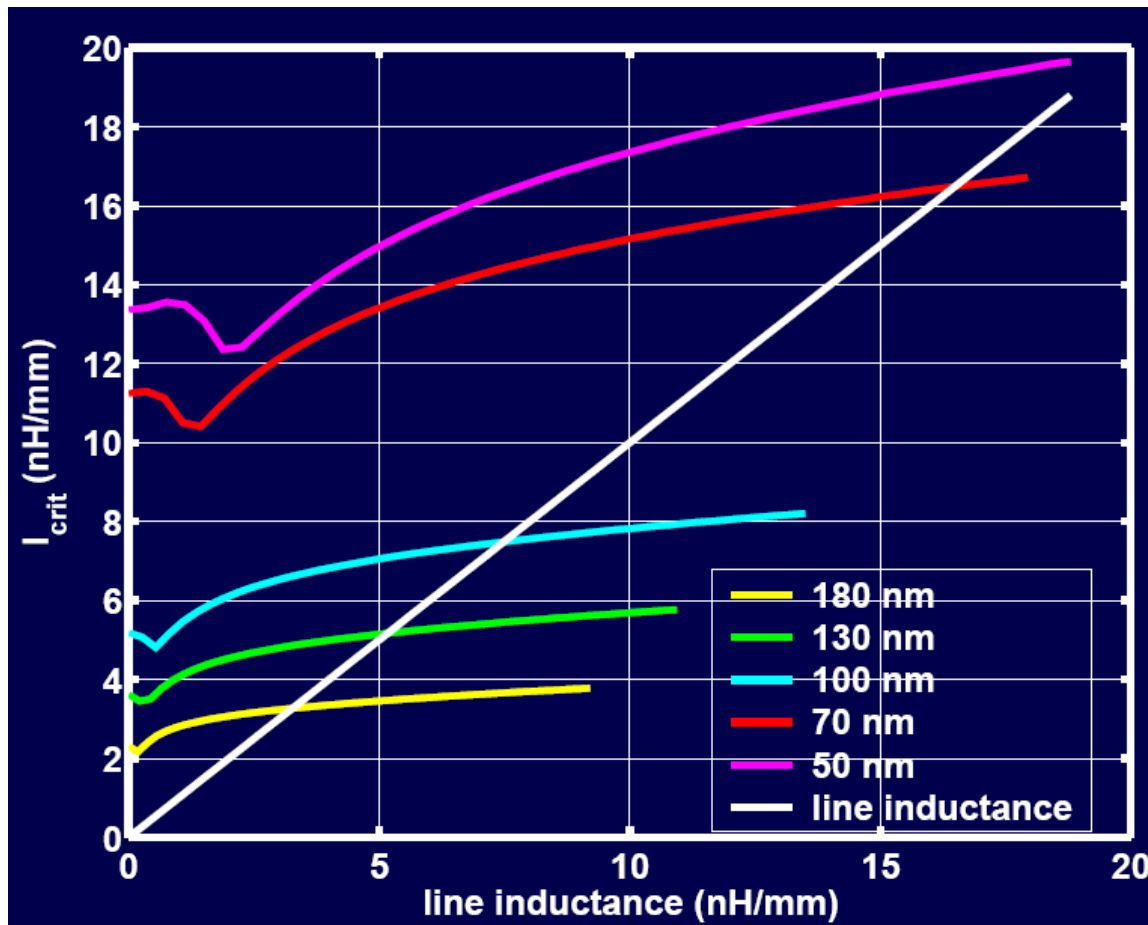
- Second order Padé expansion of $H(s)$

$$H(s) \approx \frac{1}{1 + b_1 s + b_2 s^2}$$

- System overdamped, critically damped or underdamped when $b_1^2 - 4b_2$ is $>, =, < 0$.
- At optimum buffer size and interconnect length, find l_{crit} for which the system is critically damped.
- For $l <, =, > l_{crit}$, the system is overdamped, critically damped or underdamped

Impact of Scaling: Case 1

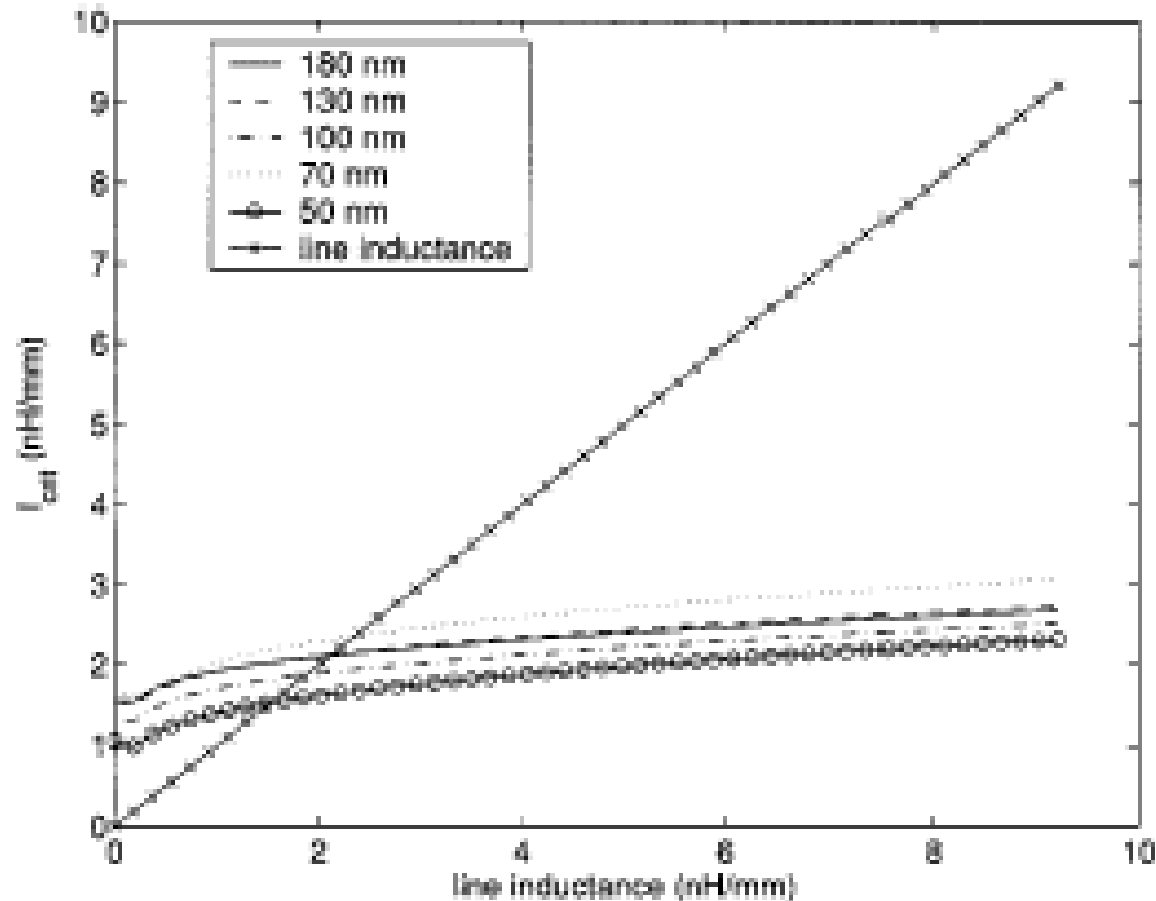
Minimum Width Global Wires



- As technology scales, $I < I_{crit}$ over larger range of line inductance
- Hence, impact of inductance **reduces** with scaling

Impact of scaling: Case 2

Unscaled Global Wires



- As technology scales, $I > I_{crit}$ over larger range of line inductance
- Hence, impact of inductance **increases** with scaling

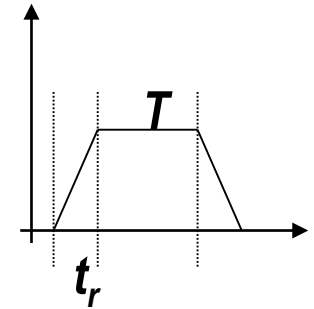
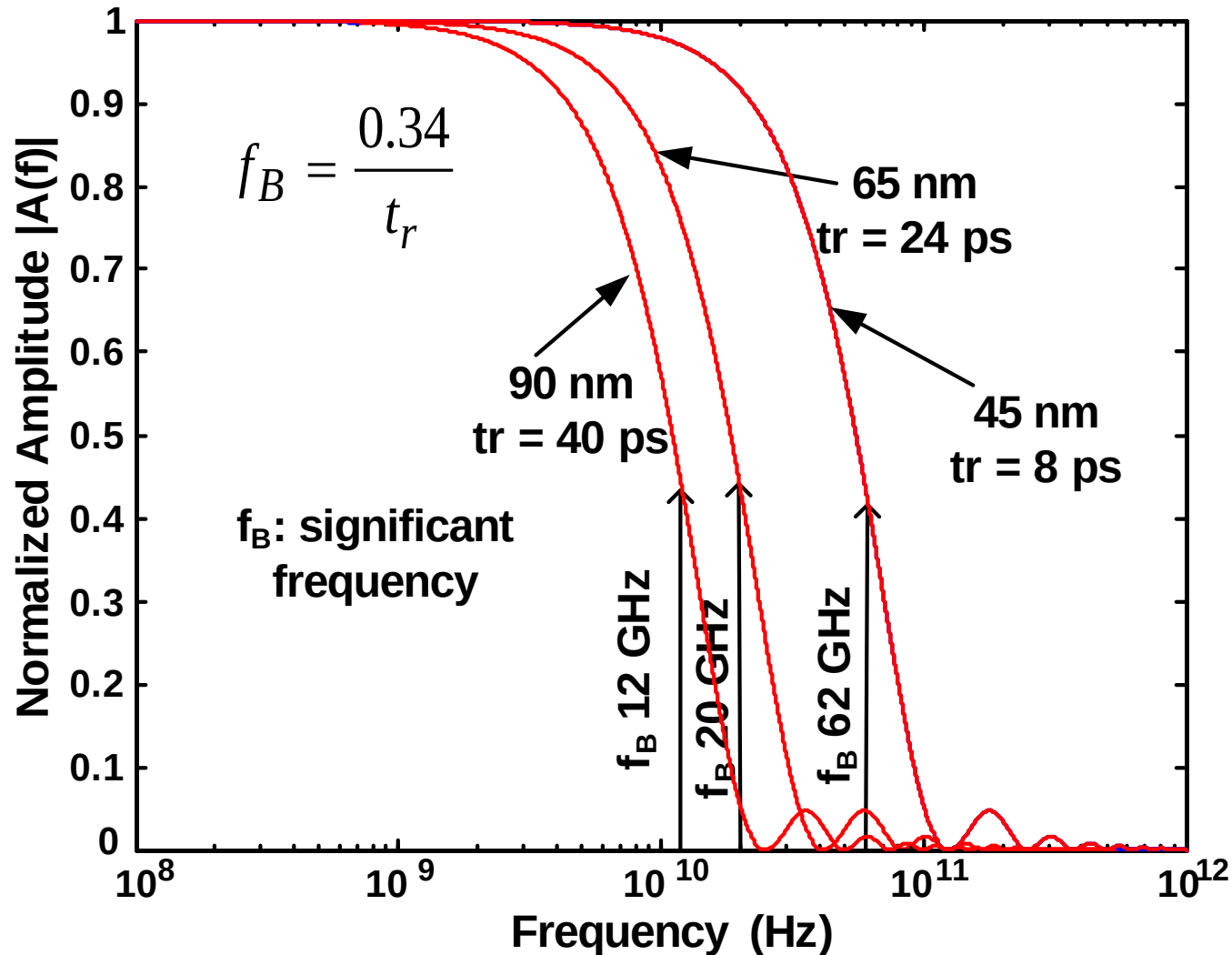
High-Frequency Issues

*K. Banerjee, S. Im and N. Srivastava, Proc. Advanced Metallization Conf., 2005.
S. Suaya, R. Escovar, S. Ortiz, K. Banerjee and N. Srivastava, Proc. Advanced
Metallization Conf., 2006.*

High-Frequency Effects

- Frequency of signals on interconnects is rising rapidly
- Frequency dependent impedance extraction is a major hurdle
 - Field solvers are unable to handle the complexity of VLSI interconnects
- Need to develop models for interconnect geometry dependent calculation of high frequency impedance

Signal Frequency on Interconnects



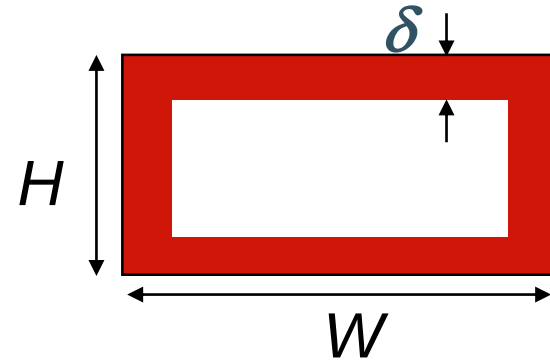
Digital signal composed of various frequency components.

Significant Frequency:

Frequency used for interconnect analysis

Frequency Dependence of R

- At high enough frequencies, R can increase due to **skin effect**
- Current flow constrained in a thin layer along the surface of the conductor: **R increases**
- The current falls off exponentially with depth into the interconnect
- **Skin depth**, δ is defined as the depth at which current falls off to a value of $1/e$ of its nominal value



$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

μ is the permeability of the surrounding dielectric

Resistance per unit length:

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H+W)}, \quad \text{for } W, H \gg \delta$$

Skin Effect

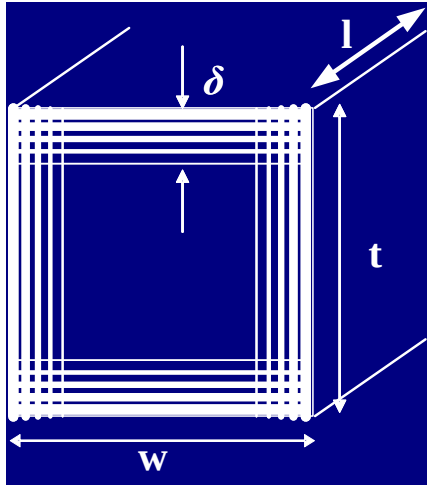
- Onset of skin effect:
at $f=f_s$, $\delta = 1/2 \times$
smallest dimension

$$f_s = \frac{4\rho}{\pi\mu(\min(W,H))^2}$$

- For Cu wires:

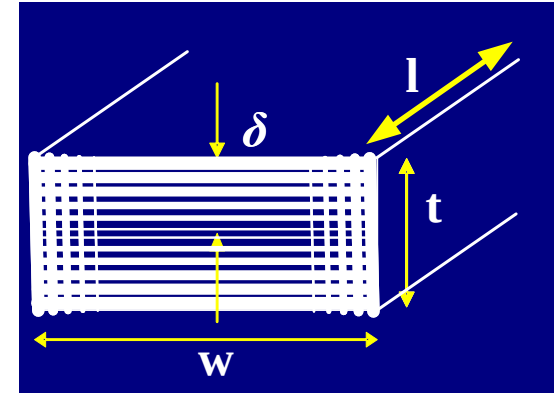
Freq	1 GHZ	5 GHZ	10 GHZ	15 GHZ	20 GHZ
Skin depth (μm)	2.08	0.93	0.66	0.53	0.46

Skin and Proximity Effects



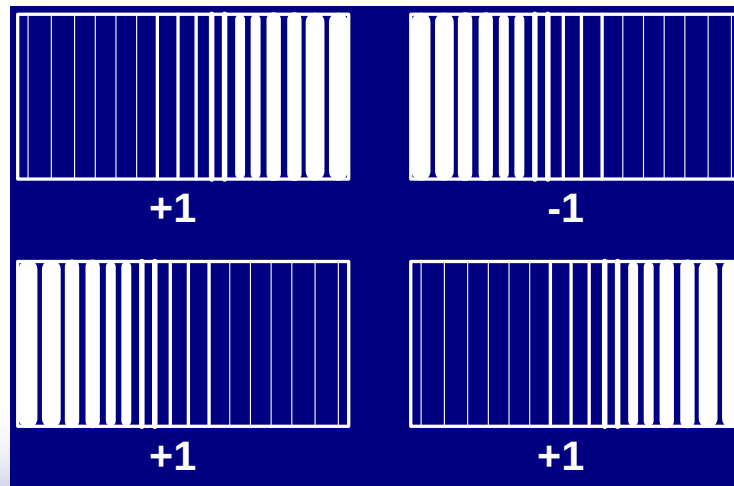
Isolated Wire $5\mu\text{m} \times 5\mu\text{m}$

Skin Effect in Isolated Conductors

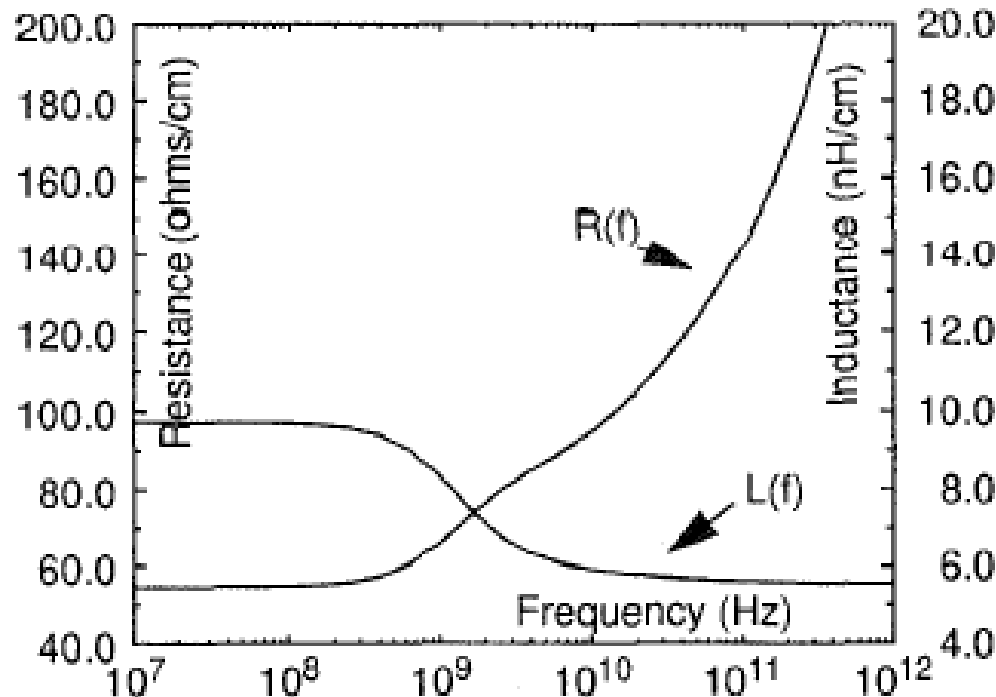


Isolated Wire $5\mu\text{m} \times 1\mu\text{m}$

Proximity Effect in Coupled Conductors



Frequency Dependence of R and L

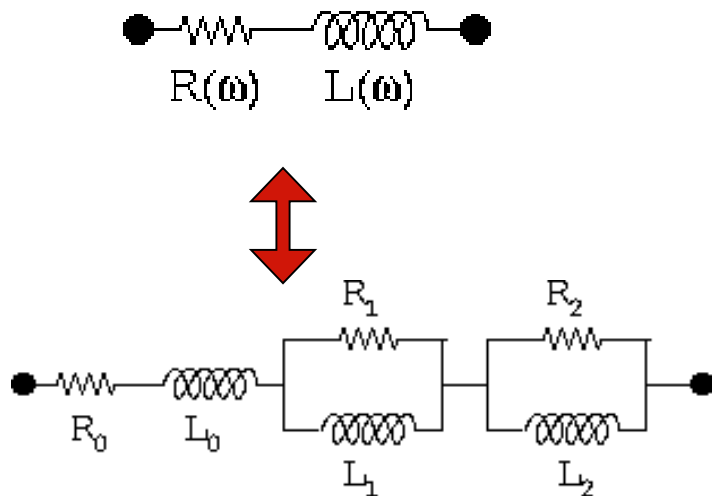


B. Krauter and S. Mehrotra, DAC, 1998.

- Resistance increases due to skin effect
- For lower frequencies, current return path is distributed between all ground lines---thus **loop inductance** is higher and return path resistance is smaller.....
- For higher frequencies, current returns through closest ground paths---thus loop area is smaller, hence loop inductance reduces and return path resistance increases

Modeling Frequency Dependent Behavior

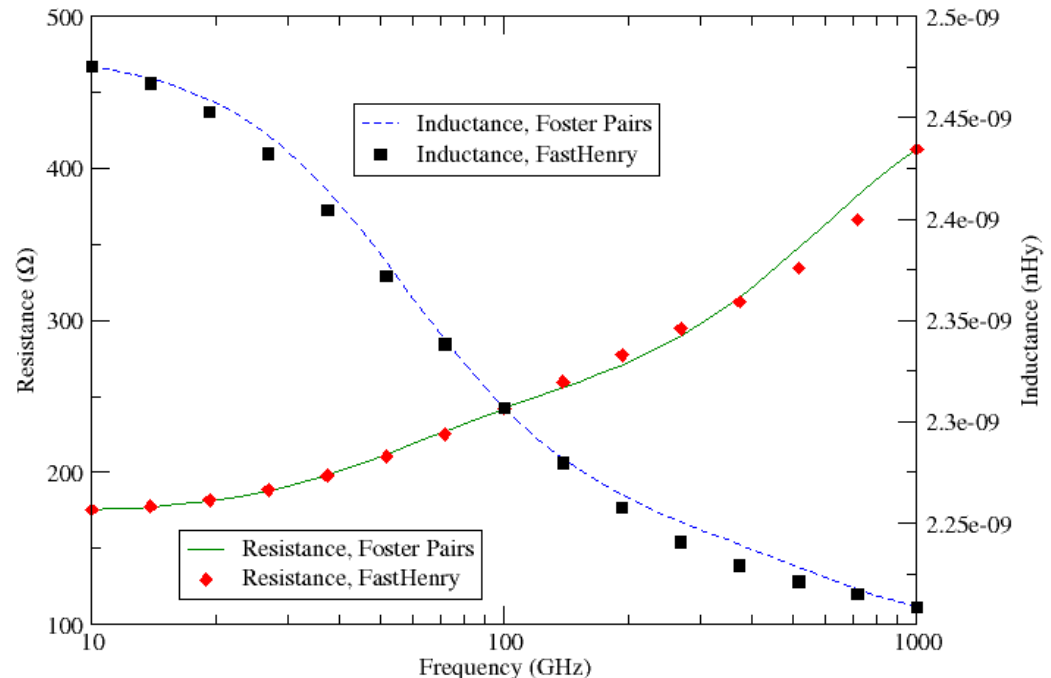
Replacing $R(\omega), L(\omega)$ with Foster Pairs



Note that at smaller frequencies L_1 ($Z=j\omega L$) will short R_1

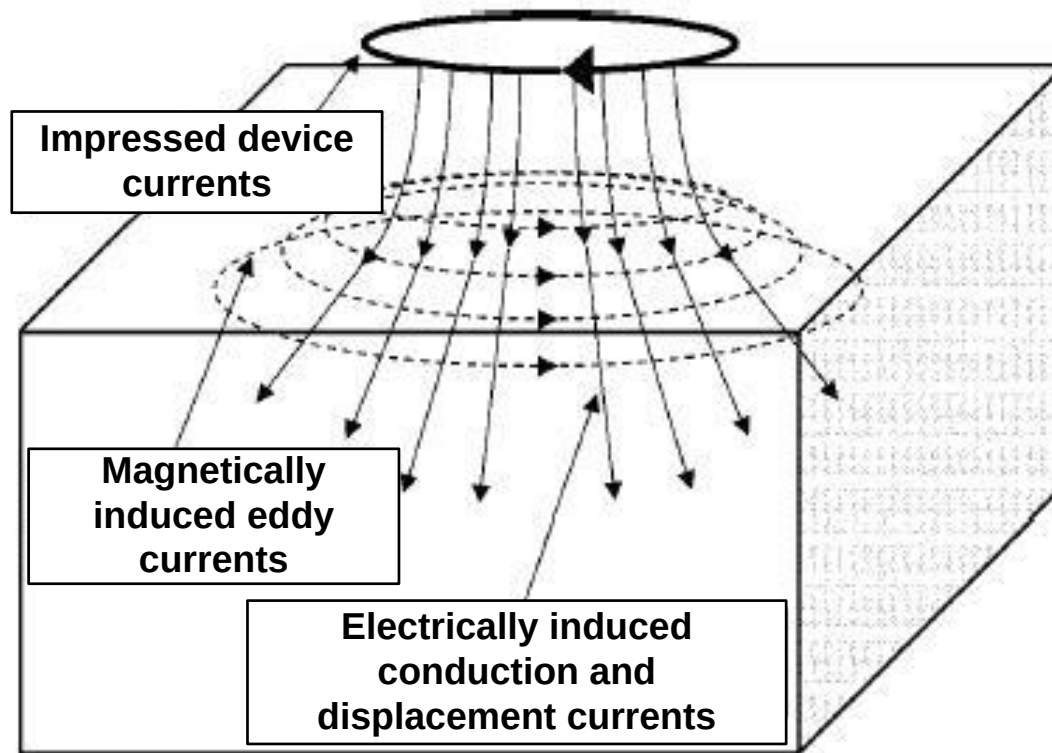
R_0 and $L_0+L_1+L_2$ are low-frequency values of R and L

At higher frequencies some current flows through R_1 and R_2 , hence R increases with frequency and effective inductance decreases



Suaya et al., Advanced Metallization Conf. 2006

Substrate Effects



*Impacts
interconnect
impedance
extraction*

A. M. Niknejad and R. G. Meyer, IEEE Trans. on Microwave Theory and Techniques, 2001