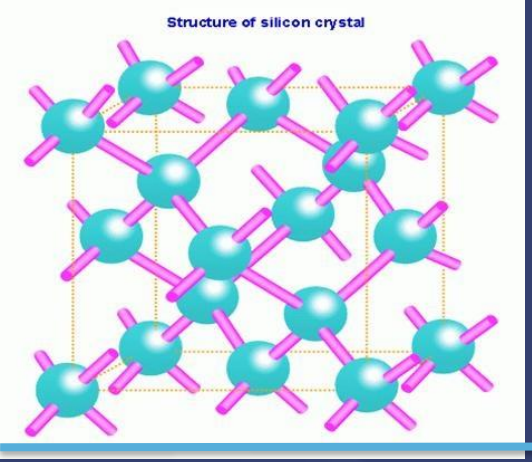
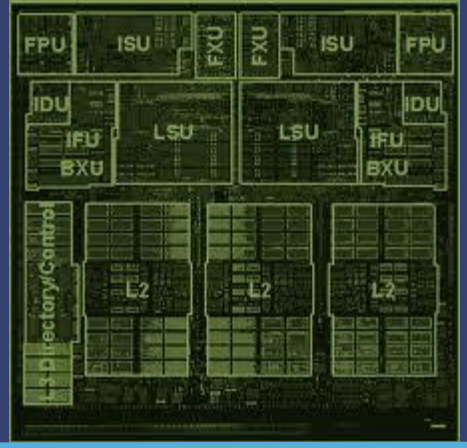
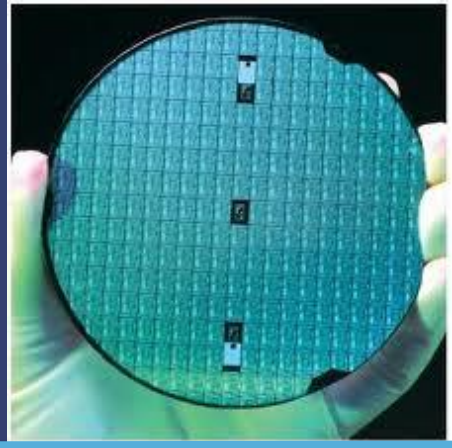






ECE 225
Lecture 5
MOSFET Scaling & Non-Classical CMOS

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara

Goals of Technology Scaling

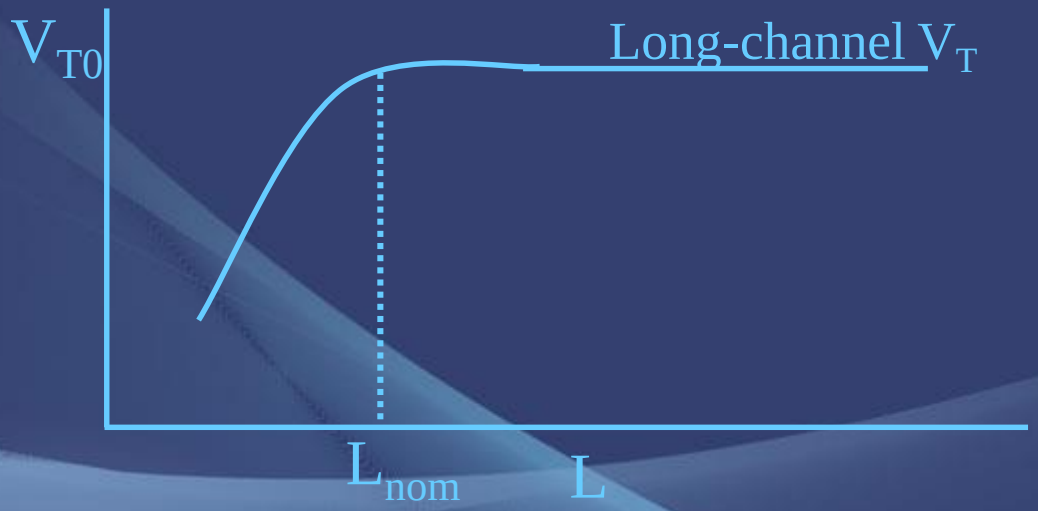
- Making things cheaper
  - Integrating more transistors per chip for the same money
  - Build same products cheaper, sell same part for less money
  - Price of fabrication of a transistor to be reduced
- But also want the transistor to be faster, smaller and low power

Short Channel Effects

- Short-channel device: channel length is comparable to depth of drain and source junctions and depletion width
  - In general, visible when L ~ 1μm and below
- Short-channel effects
  - Carrier velocity saturation
  - Mobility degradation
  - Threshold voltage variation
  - Oxide breakdown
  - Avalanche breakdown

Threshold voltage Roll-off…

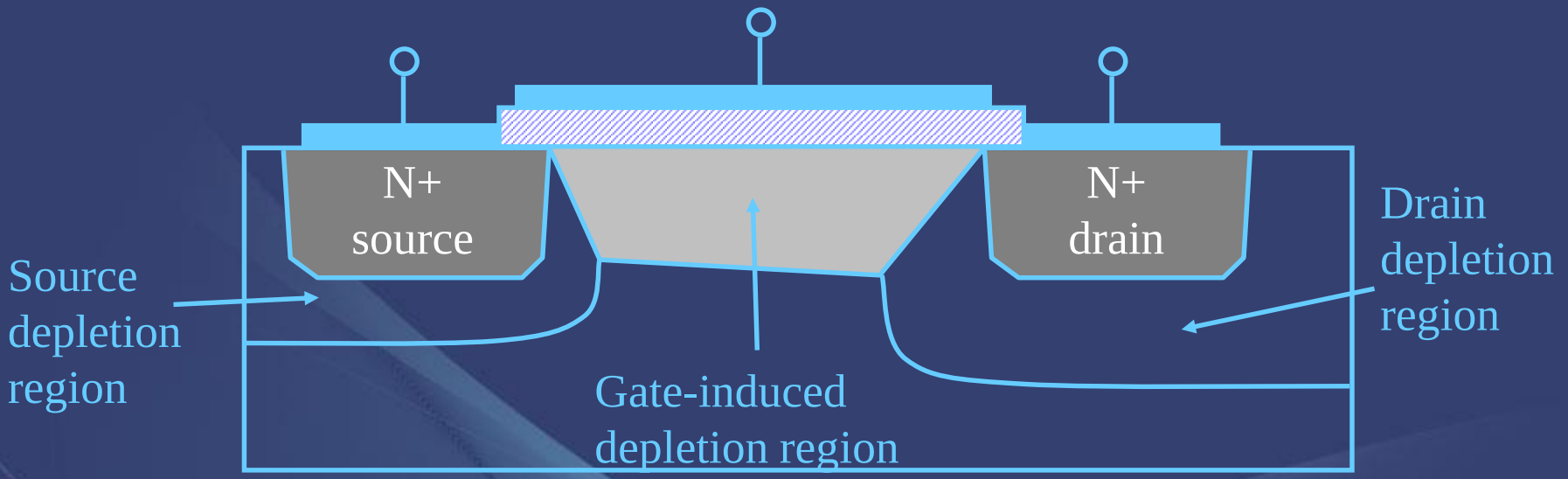
Graphically: V_{T0} versus channel length L



V_T Roll-off:

V_T decreases rapidly with channel length

Reason for V_T Roll-off....



- Even with V_{GS}=0, part of the channel is already depleted
- Bulk depletion charge is smaller in short-channel device → V_T is smaller

Estimation of V_T Roll-off….

- Change in V_{t0}:
  - x_{dS}, x_{dD}: depth of depletion regions at S, D
  - x_j: junction depth

$$\Delta V_{t0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A\left|2\phi_F\right|} \bullet \frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right]$$

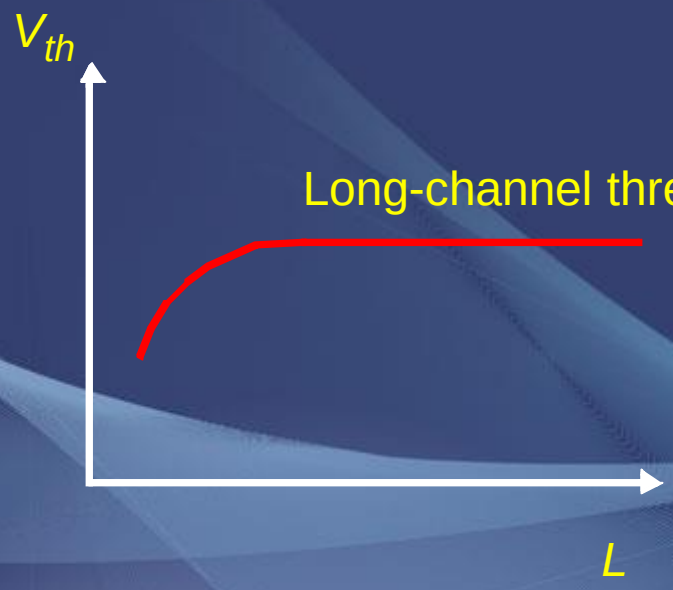
- ΔV_{t0} is proportional to (x_j/L)
  - For short channel lengths, ΔV_{t0} is large
  - For large channel lengths, term approaches 0

DIBL

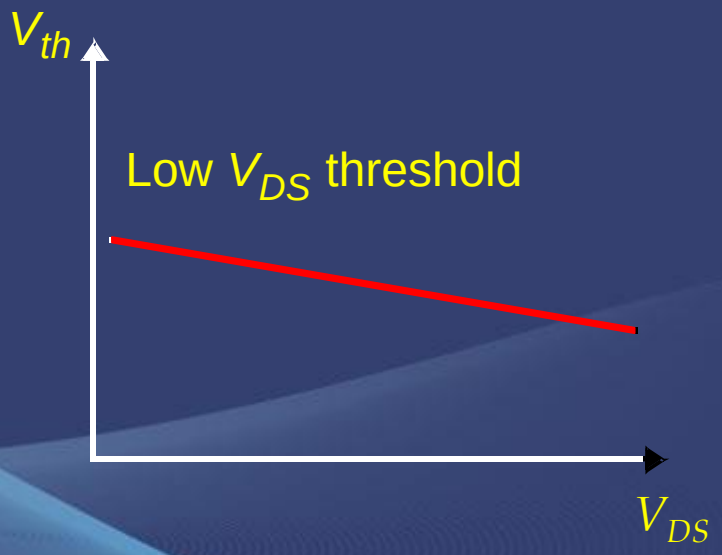
- Drain-induced barrier lowering (DIBL)
  - Drain voltage V_{DS} causes change in threshold voltage
  - As V_{DS} is increased, threshold voltage decreases
- Cause: depletion region around drain
  - Depletion region depth around drain depends on drain voltage
  - As V_{DS} is increased, drain depletion region gets deeper and extends further into channel
  - For very large V_{DS}, source and drain depletion regions can meet → *punch-through*!
- Issue: results in uncertainty in circuit design

Effect of SCE and DIBL on Vth…..

- $V_{th} = V_{th\_long\text{-}channel} - SCE - DIBL$



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (DIBL) (for low L)

Threshold Voltage Variation

Short-channel effects cause threshold voltage variation:

- V_t rolloff
  - As channel length L decreases, threshold voltage decreases
- Drain-induced barrier lowering
  - As drain voltage V_{DS} increases, threshold voltage decreases
- Hot-carrier effect
  - Threshold voltages drift over time
- Negative-Bias Temperature Instability (NBTI)
  - Issue in PMOS transistors
  - Vt drifts over time
  - Typical stress temperature 100-150 C
  - Typical oxide electric fields of 5-6 MV/cm

Subthreshold Leakage

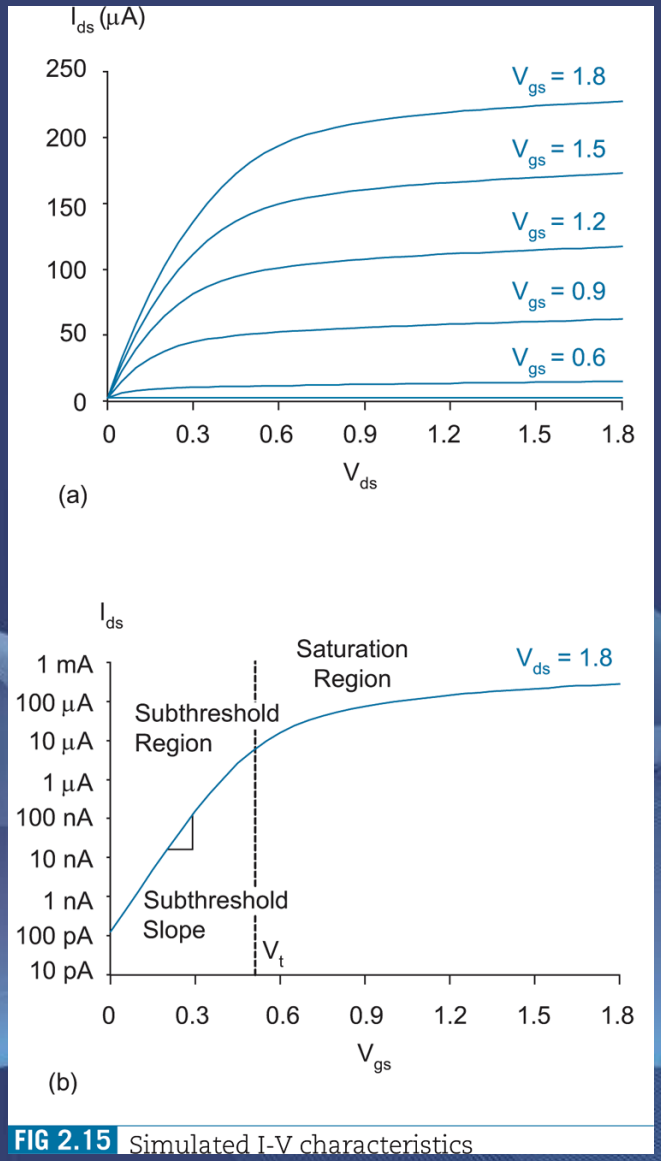


FIG 2.15 Simulated I-V characteristics

- *Dominant leakage mechanism*
- *Increases exponentially with temperature and Vt reduction*

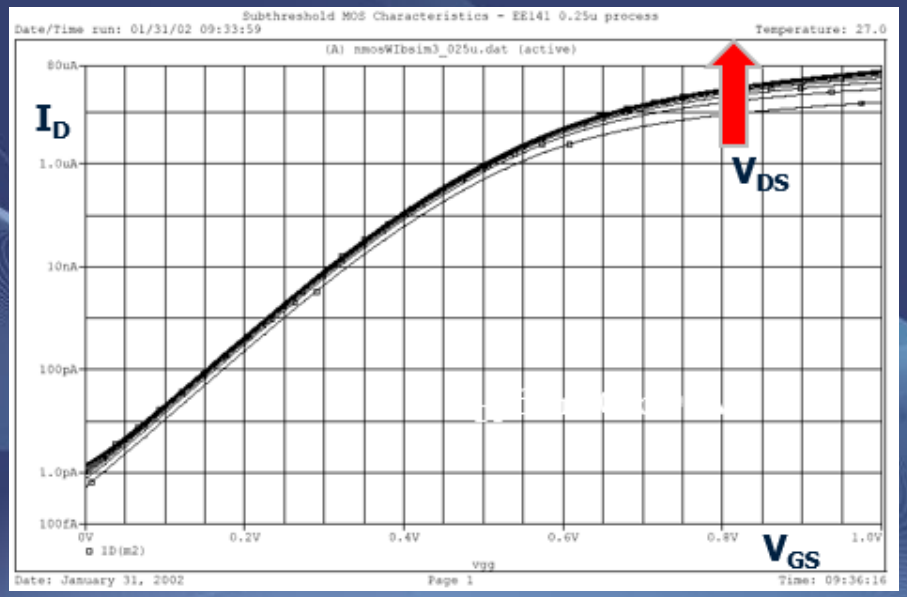
$$I_D(subthreshold) = I_S W e^{\frac{q}{kT}(AV_{GS} + BV_{DS})}$$

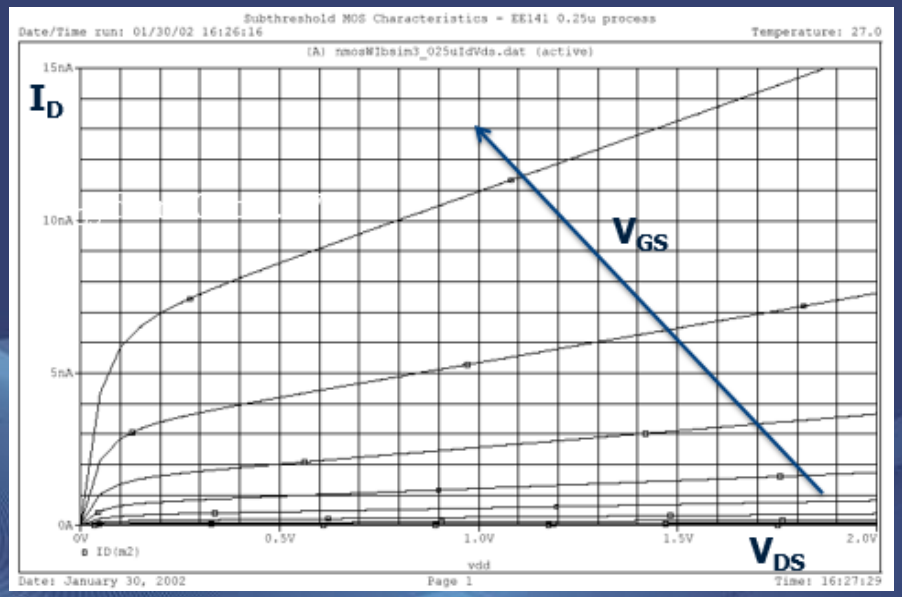
$$S = \left(\frac{d(\log I_d)}{dV_g}\right)^{-1} = \left(\frac{\partial V_g}{\partial \psi_s}\right)\left(\frac{\partial \psi_s}{\partial(\log I_d)}\right) = \left(1 + \frac{C_{dm}}{C_{ox}}\right)\frac{kT}{q}\ln(10)$$

Typical values for S: 60 - 100 mV/decade

Sub-Threshold I_D vs V_{DS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)\left(1 + \lambda \cdot V_{DS}\right)$$





Avalanche Breakdown

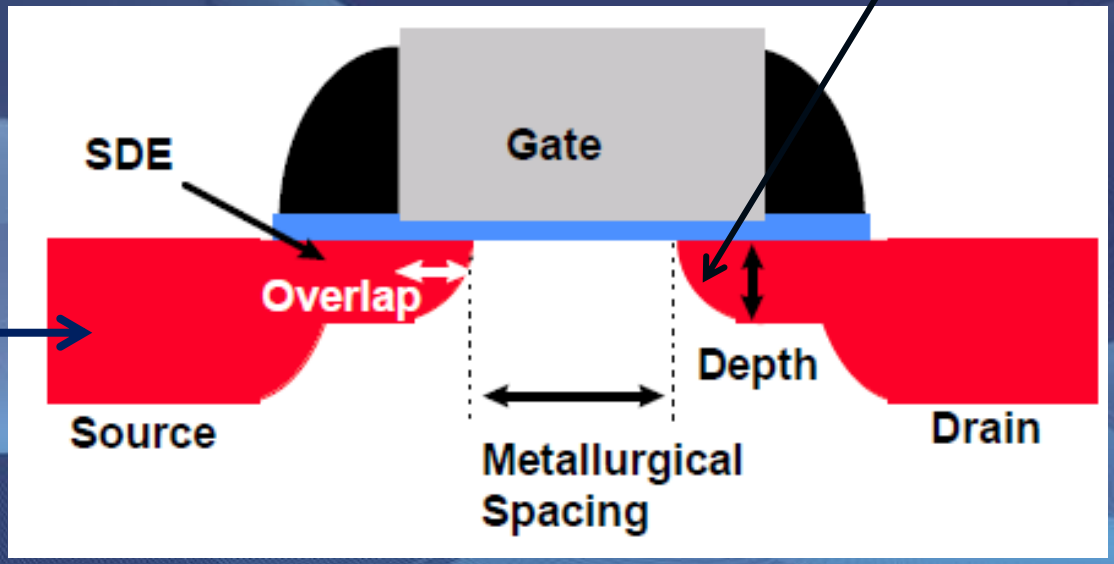
- Due to scaling, high-velocity electrons can impact the drain, dislodging holes---Called impact ionization
- Holes are swept towards grounded substrate → cause substrate current
- Also affects long-term reliability
- This is another factor which limits the process scaling → voltage must scale down as length scales

S/D Engineering in the Scaled Regime

- Scaling of S/D extension (SDE) depth and gate overlap
- Junction depth in 0.25 um technology node is 50-100 nm.

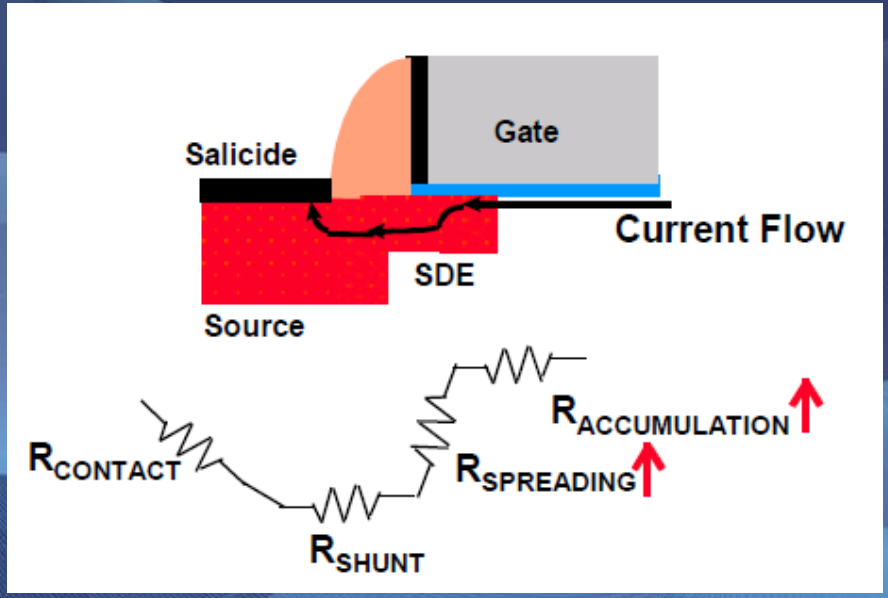
Lightly doped region to lower electric field and prevent hot-electrons

Heavy doping needed for the S/D contact and for lowering the sheet resistance



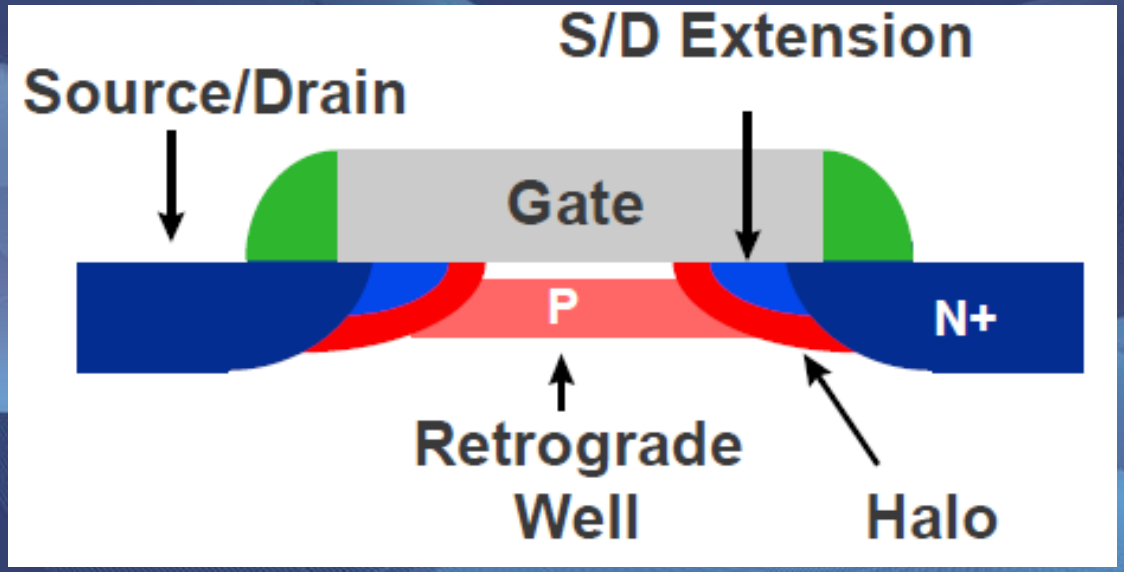
S/D Engineering

- Shallow junctions lead to high external resistance (sheet resistance is higher)
- Shallow junction improves the short channel characteristics by reducing the amount of charge controlled by the drain (note that gate has less control in regions further from the oxide/Si interface)



Channel Engineering

- Modifying doping profile in the channel:
  - Retrograde doping (for better electrostatics – well region has lower drain control; and to prevent punchthrough, since depletion width is smaller)
  - Halo doping (increases junction abruptness--- good for electrostatics and preventing punchrhrough)



Gate Leakage

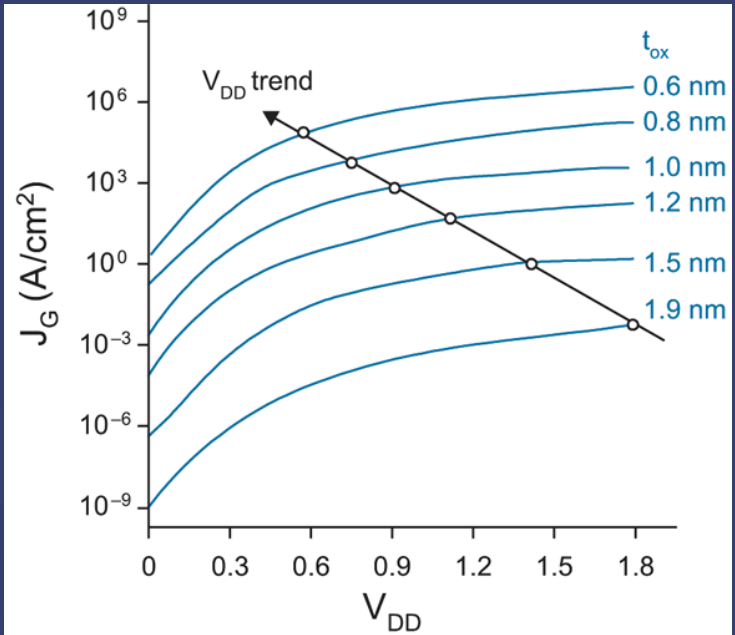
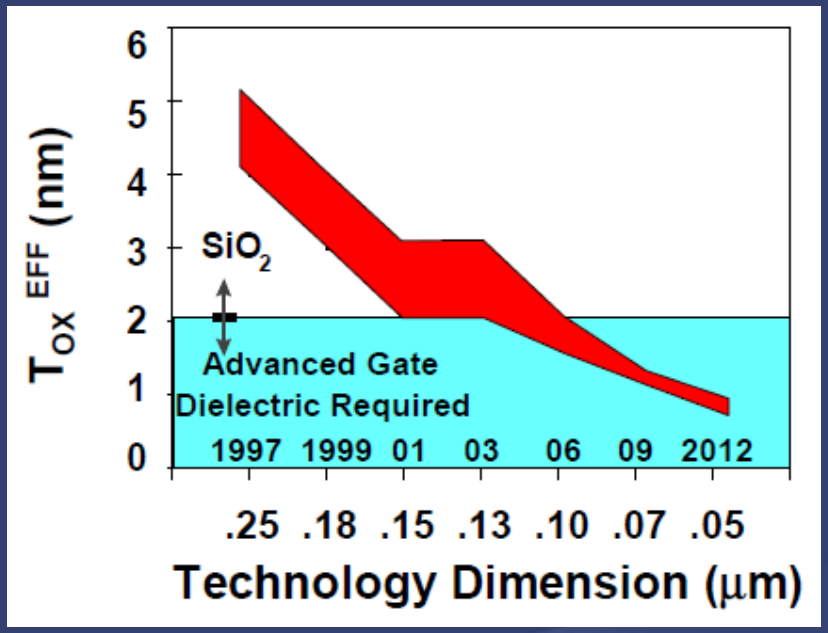
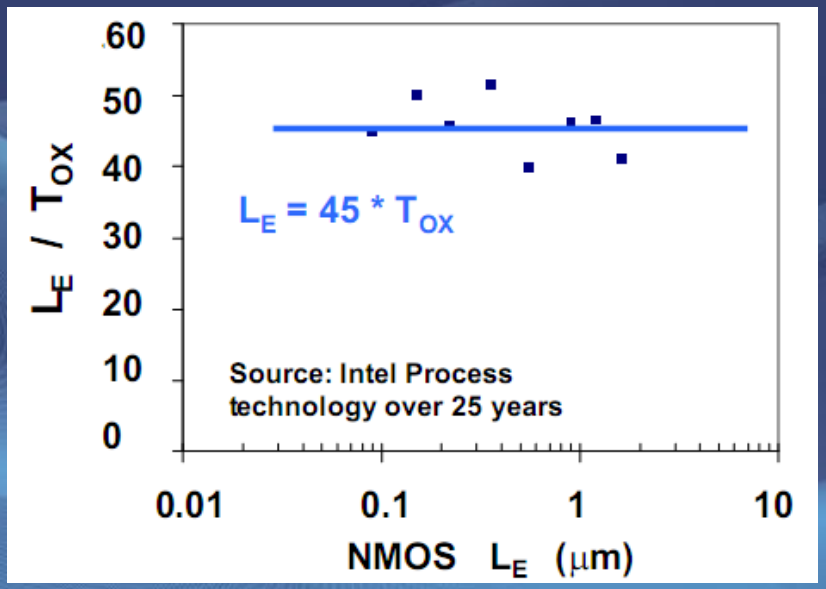


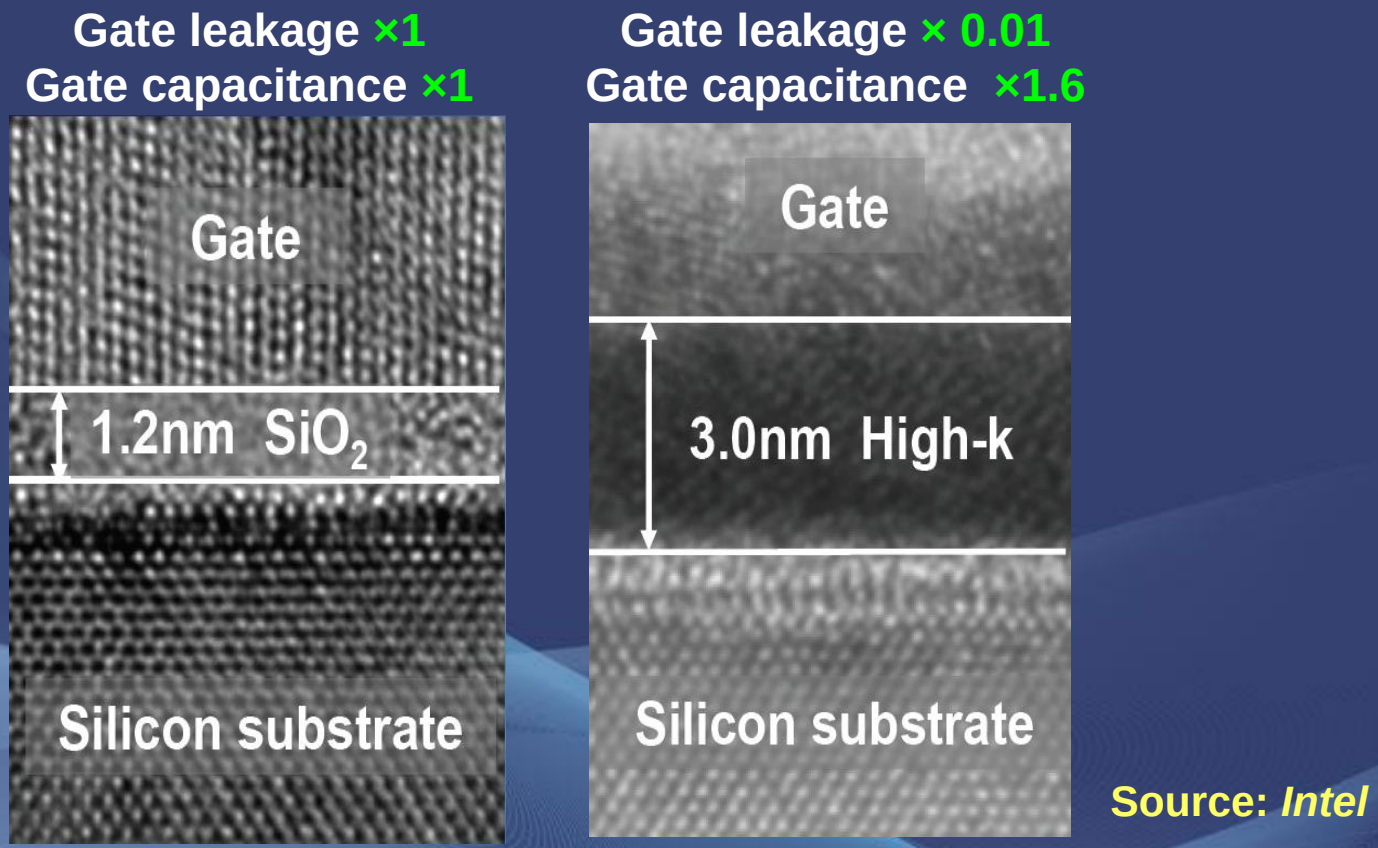
FIG 2.20 Gate leakage current from [Song01]





- *Increases with gate oxide (SiO2) scaling*
- *High-k gate oxides can be used to lower gate leakage*
- *Independent of temperature*

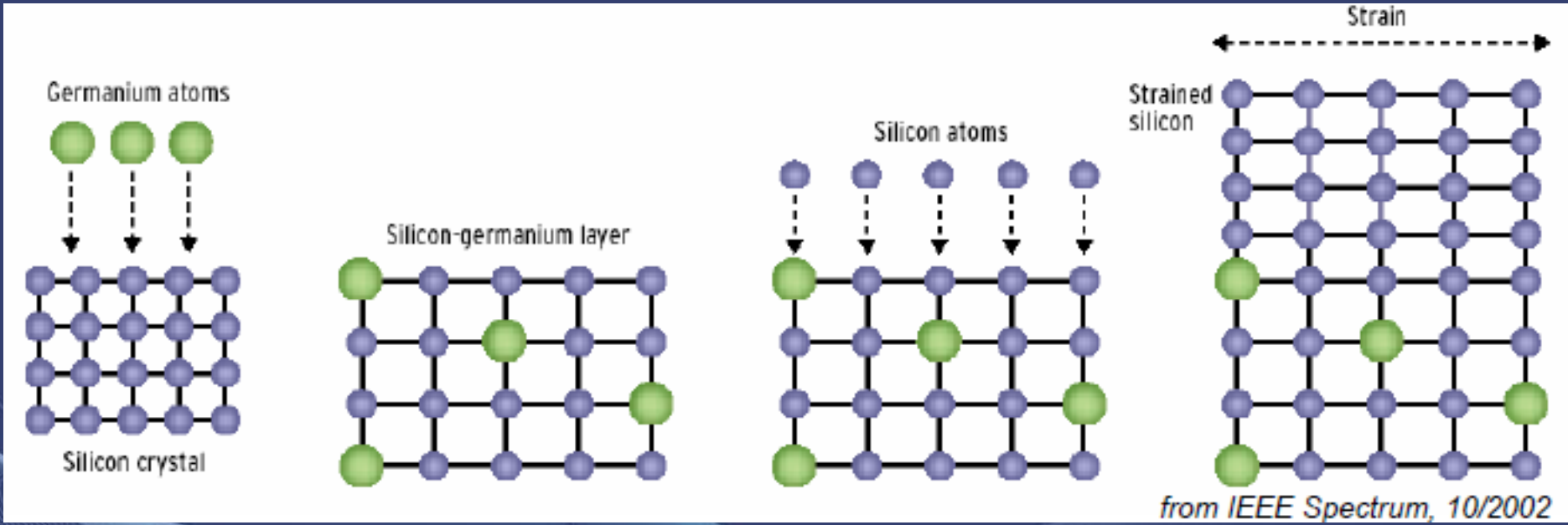
High-k/Metal Gate Technology



Source: *Intel*

- High-k/metal gate devices offer lower gate leakage with small increase in gate capacitance

Strained Silicon MOSFET

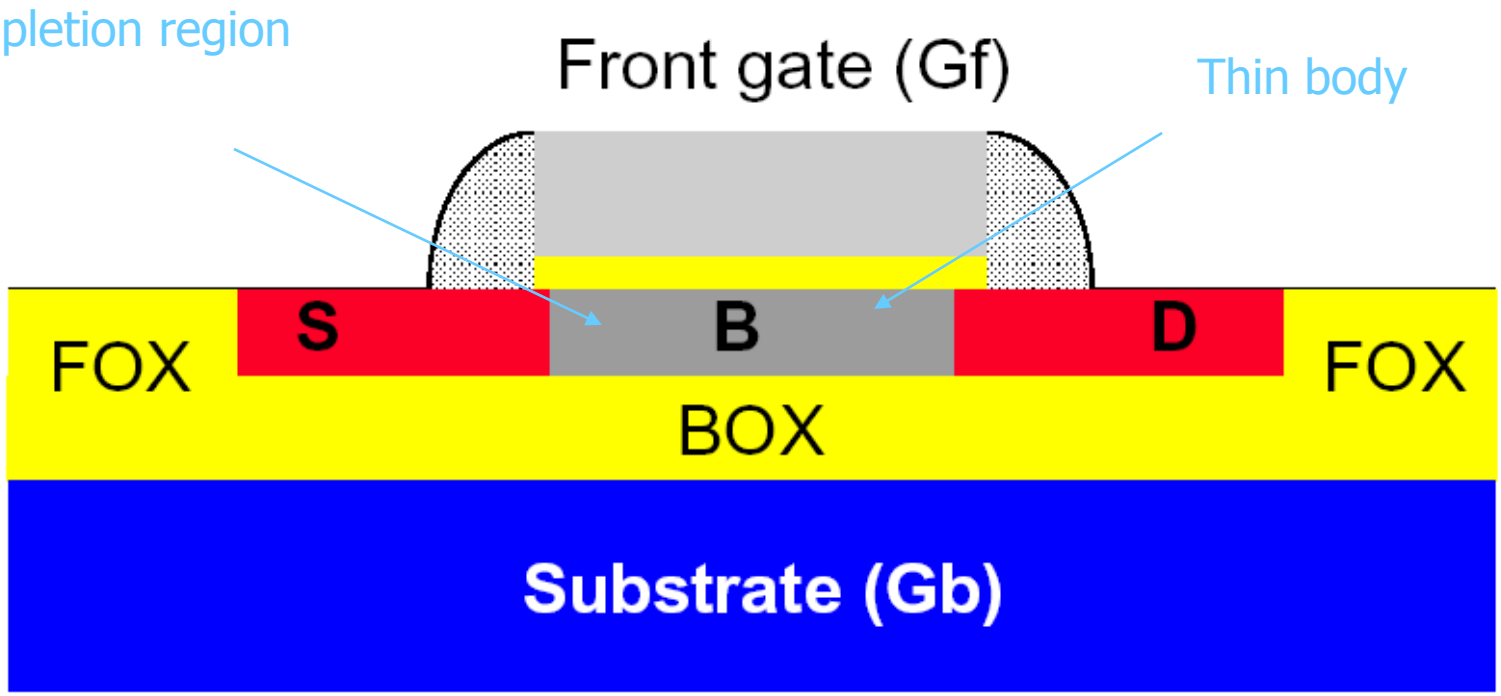


- Silicon in channel region is strained in two dimensions by placing a Si-Ge layer underneath (or more recently adjacent to) the device layer
- Strained Si results in changes in the energy band structure of conduction and valence band, reducing lattice scattering
- Benefit: increased carrier mobility, increased drive current (drain current)

Non-classic CMOS Devices

SOI

basic structures



Fully depleted (FD) body

Another View

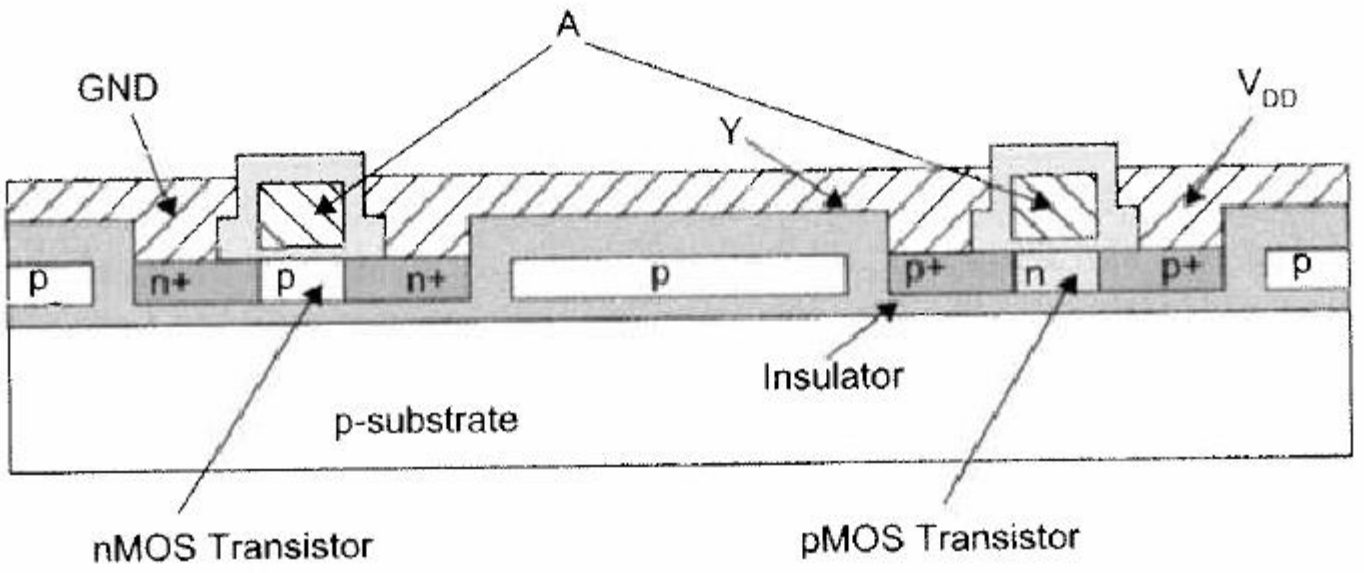
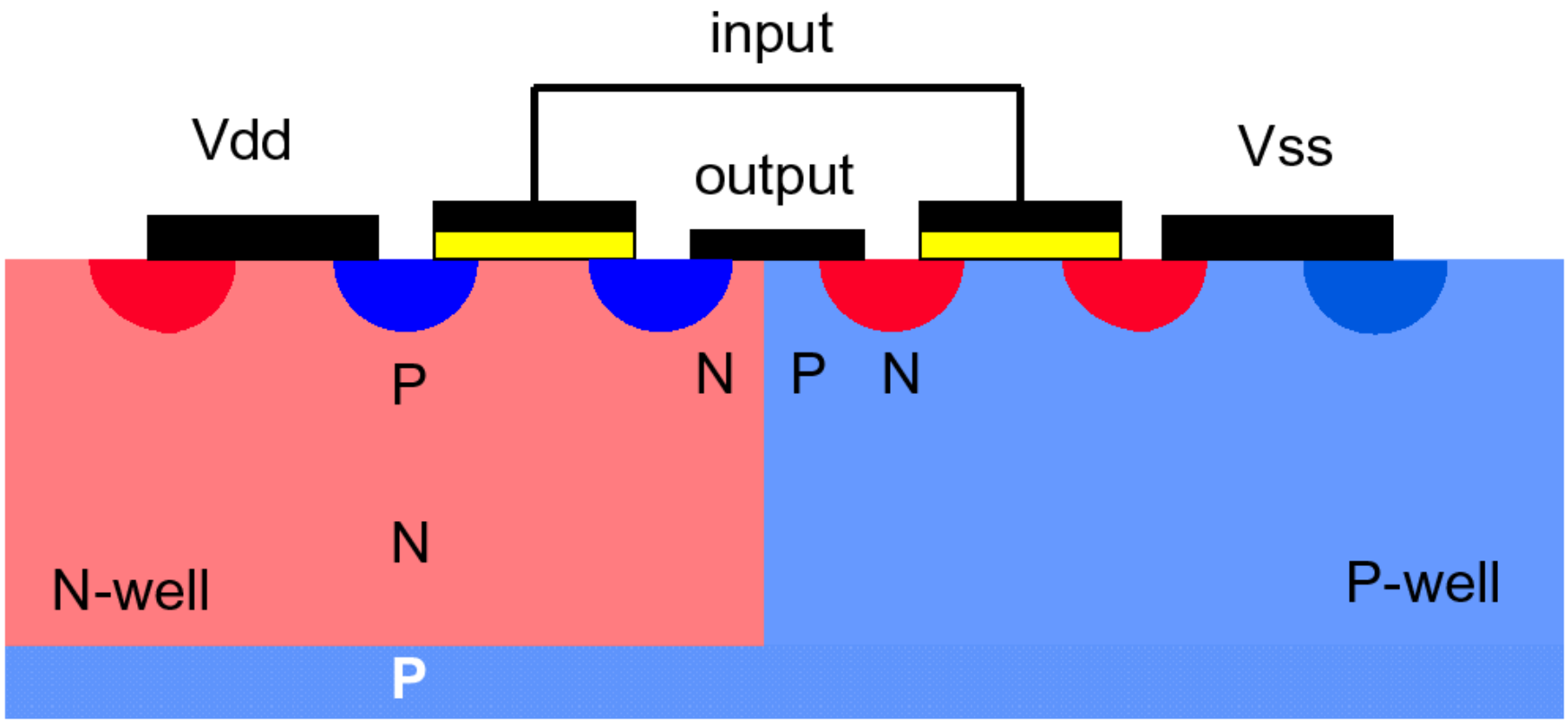


FIG 6.69 SOI inverter cross-sections

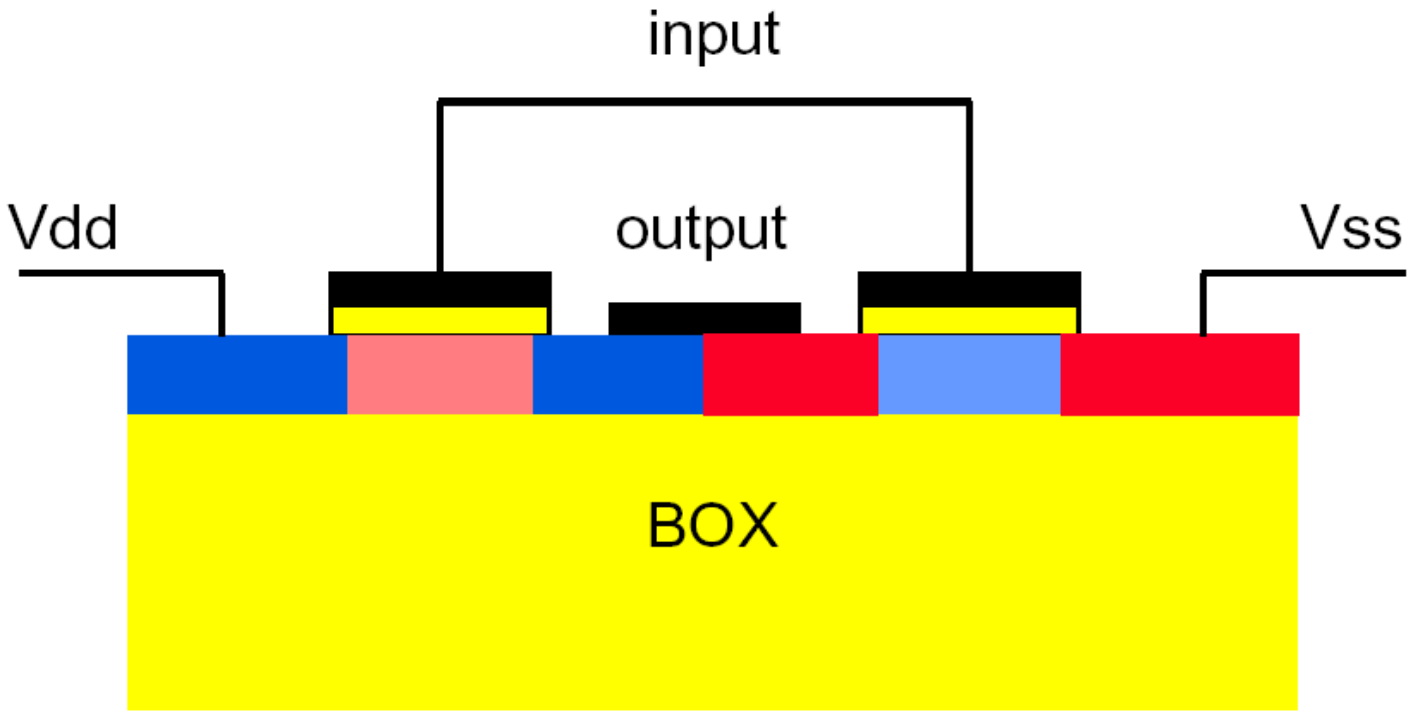
Source: Weste/Harris

benefits of SOI



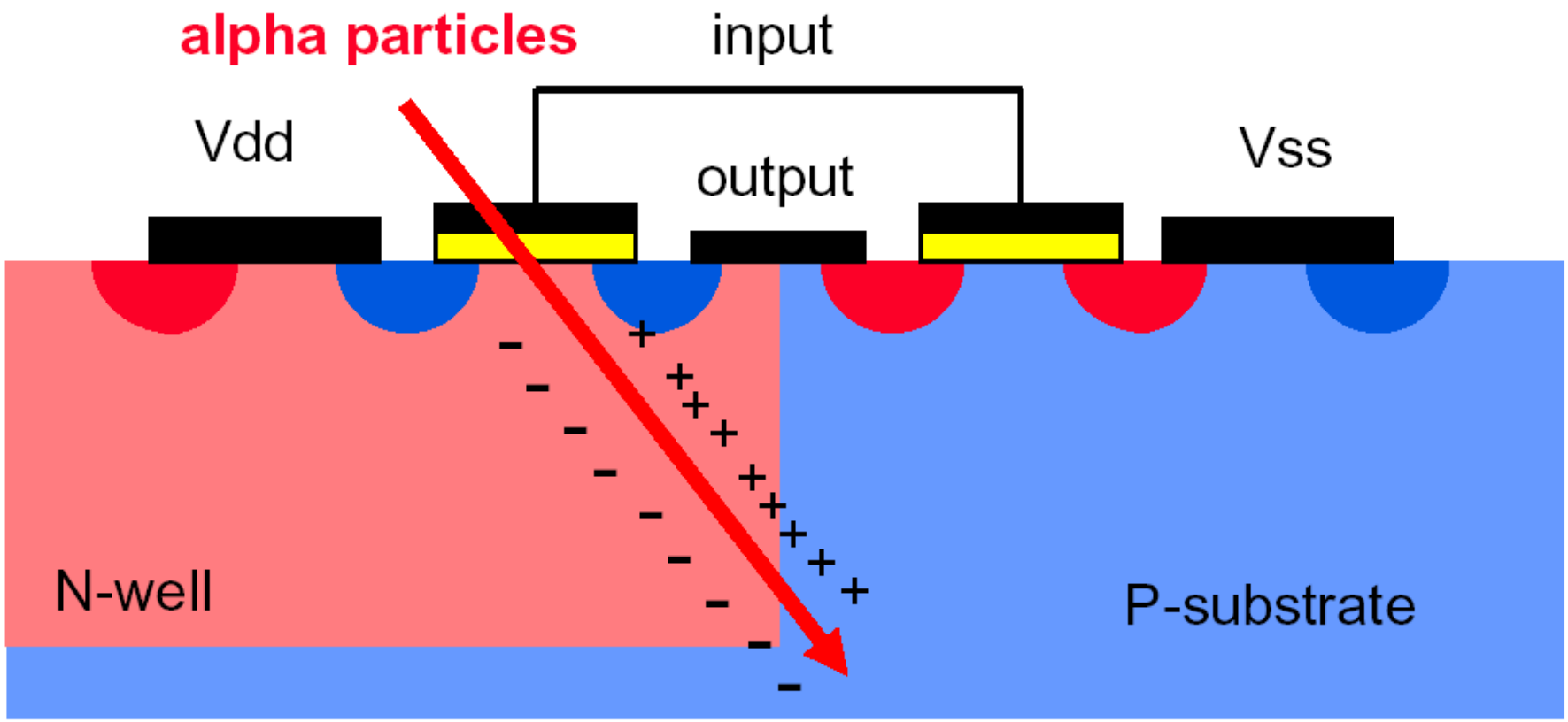
Parasitic bipolar devices → “latchup”

benefits of SOI



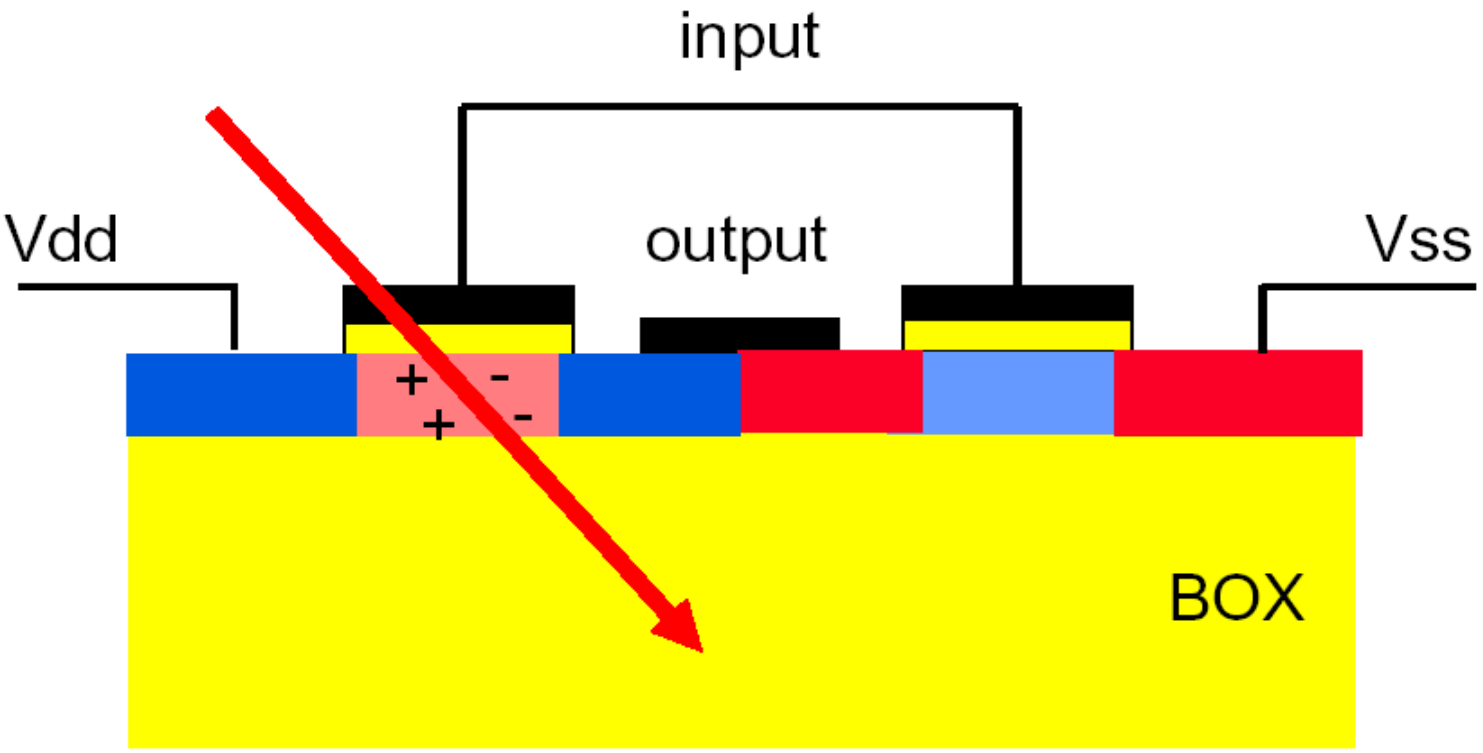
No parasitic bipolar devices ➡ no latchup

soft errors in bulk CMOS



Alpha particles → "soft" errors

soft errors in SOI

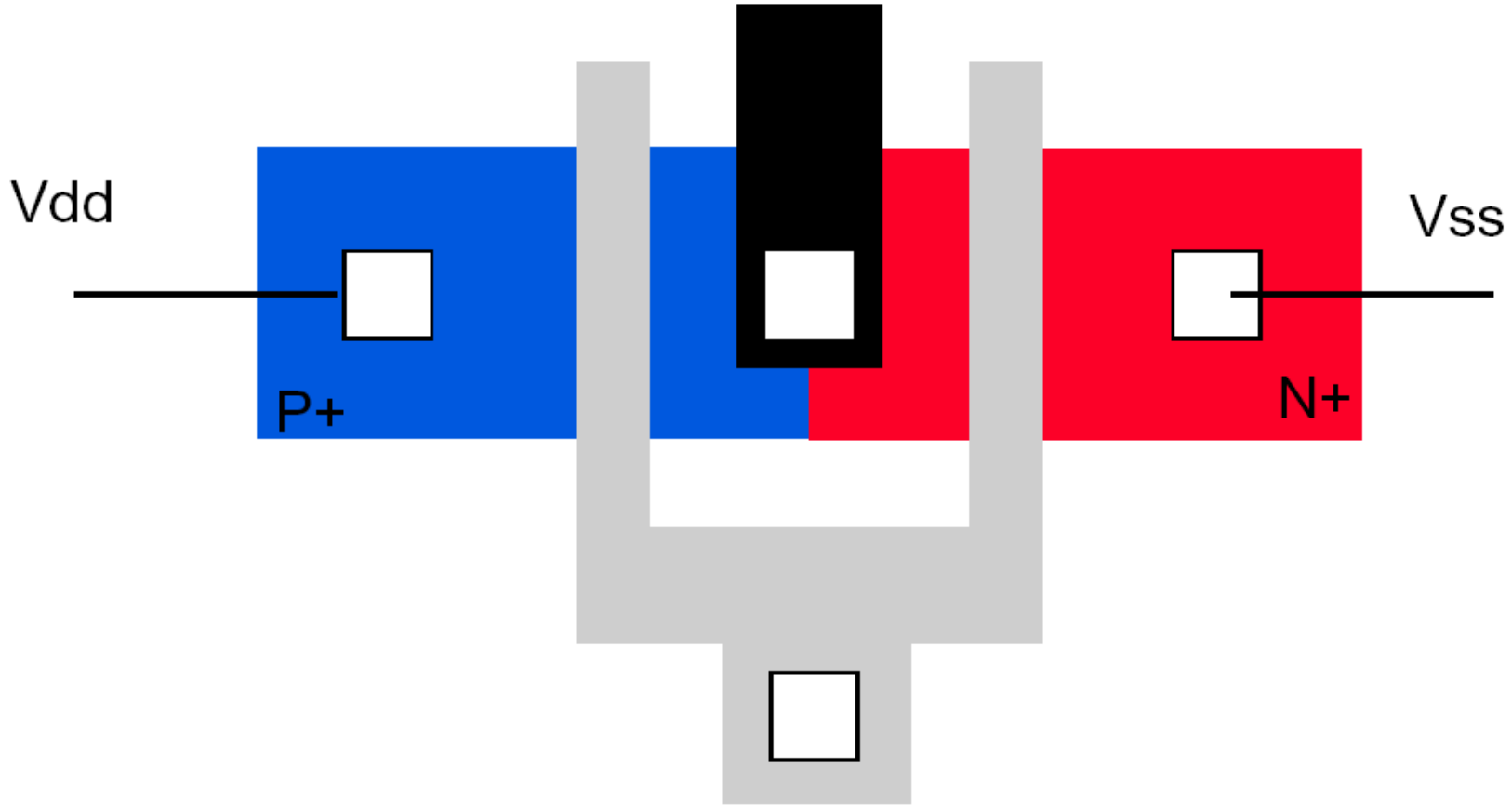


Not as much substrate to generate charge in!

Low soft error rate

layout for bulk CMOS

layout for SOI



Simpler isolation → simpler process → smaller layout

benefits of SOI

-Simple IC processing (isolation)

-Higher density

-Reduced S/D junction capacitance (speed/power)

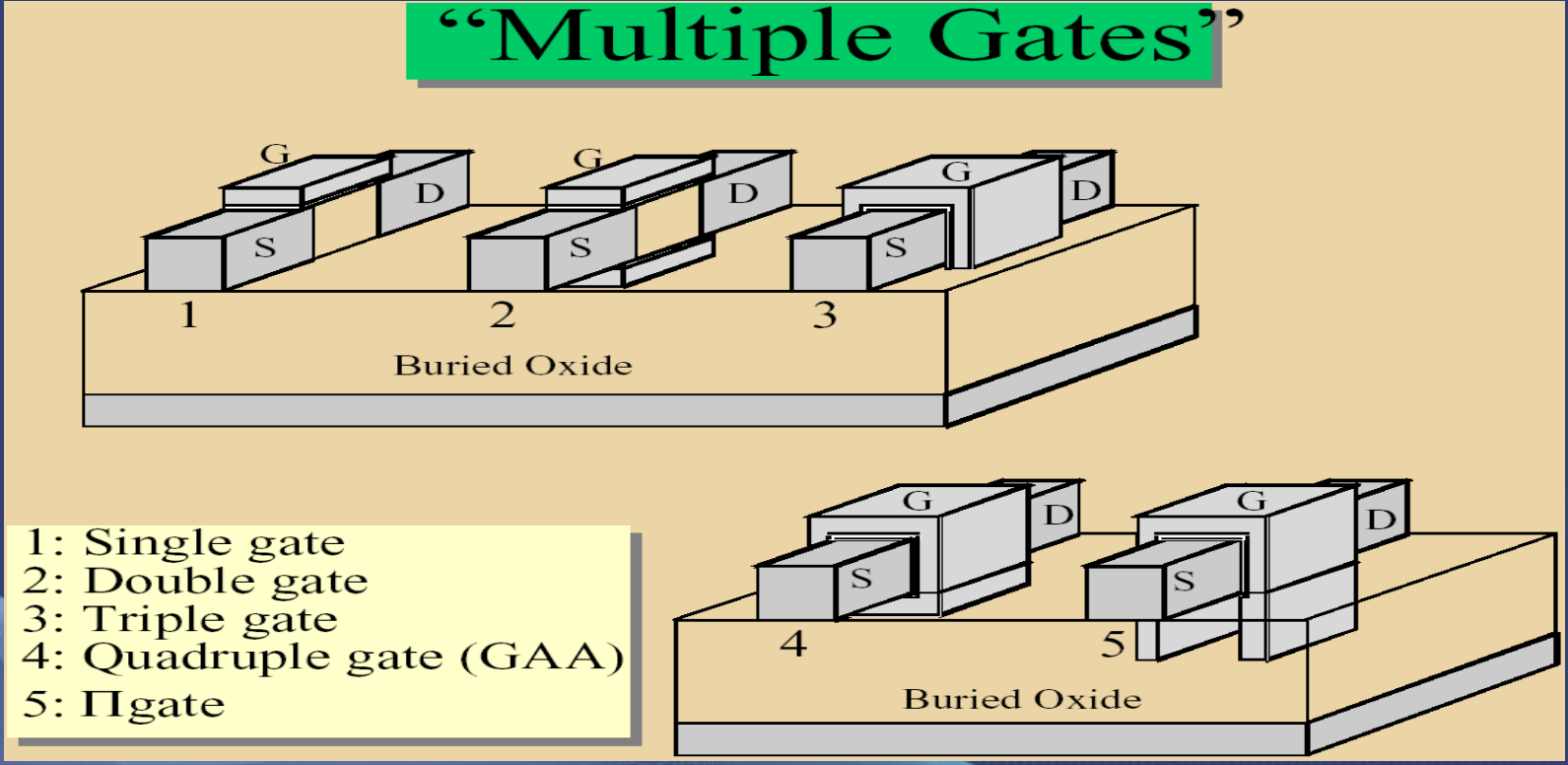
-Low soft-error rate

-No latch-up

-No (normal) body effect

SOI -> Multigate FET

Why Multi-Gate MOSFETs ?



- Higher current drive => better performance
- Prophesized to show higher tolerance to scaling
- Better integration feasibility, raised source-drain structure, ease in integration
- Larger number of parameters to tailor device performance

Device Design (Electrostatics)

Single gate	$\lambda_1 = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si}\, t_{ox}}$
Double gate	$\lambda_2 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si}\, t_{ox}}$
Quadruple gate (square section)	$\lambda_4 \cong \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}} t_{si}\, t_{ox}}$
Surrounding gate (circular section)	$\lambda_o = \sqrt{\frac{2\varepsilon_{si}\, t_{si}^2\, \ln\left(1 + \frac{2\, t_{ox}}{t_{si}}\right) + \varepsilon_{ox}\, t_{si}^2}{16\, \varepsilon_{ox}}}$

λ: natural length-- an indicator of device scaling ability.

L_{eff} > 2.5λ is the bottom line to sustain an acceptable electrostatics.

What does FinFet look like?

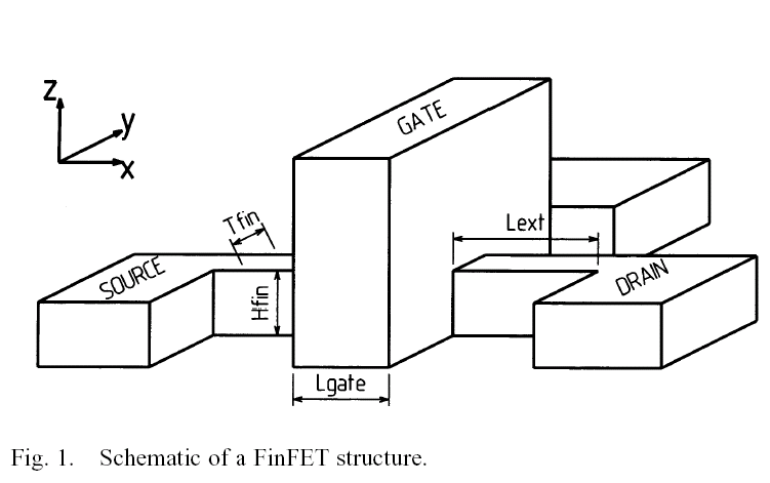
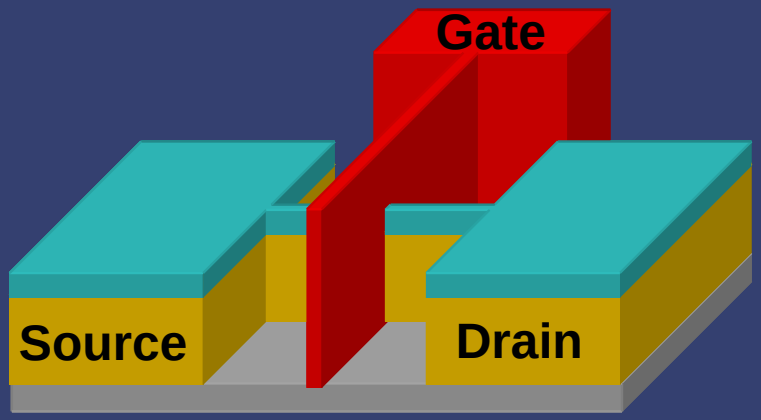
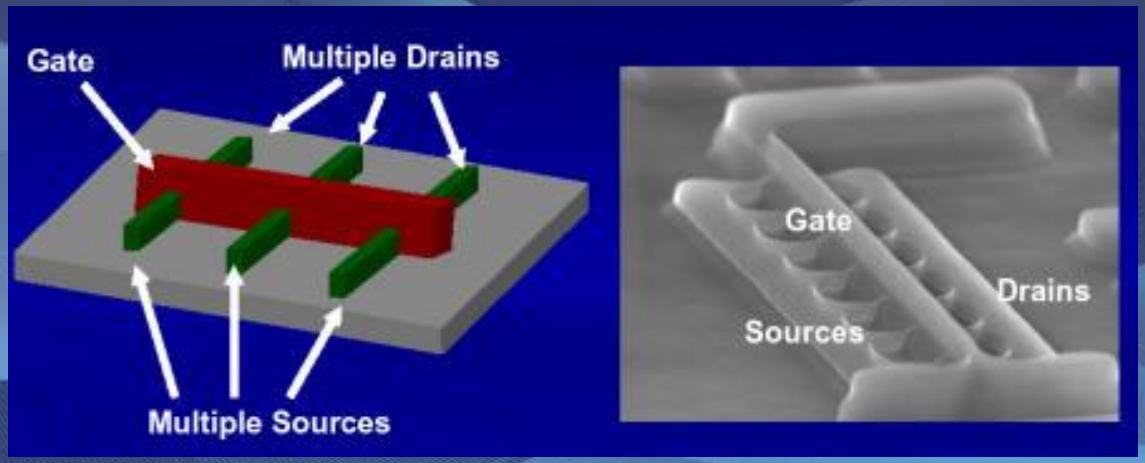


Fig. 1. Schematic of a FinFET structure.

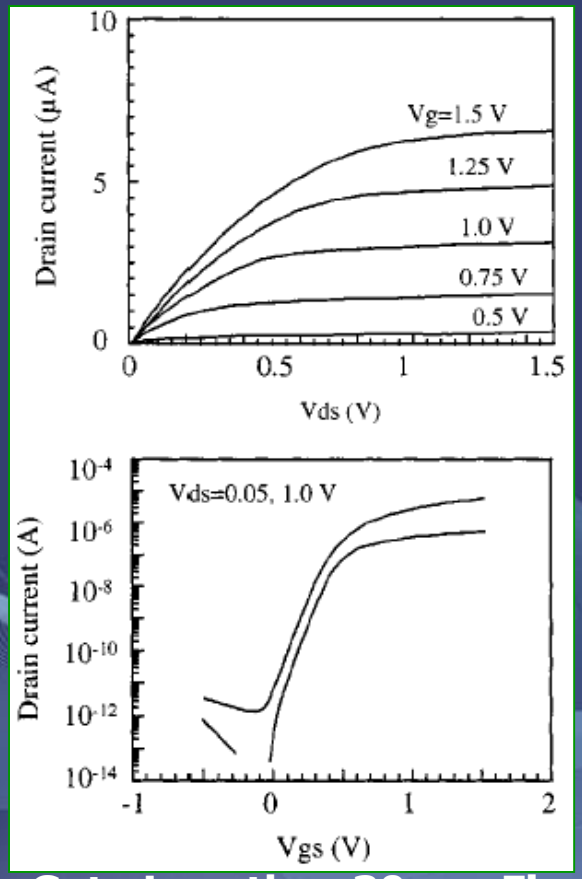


3D view of FinFET

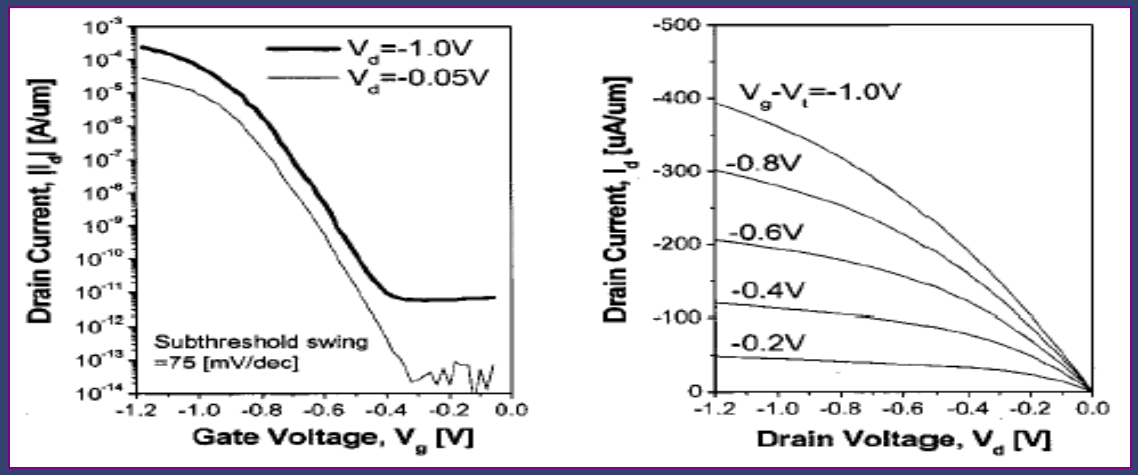


3D view of multi-fin FinFET

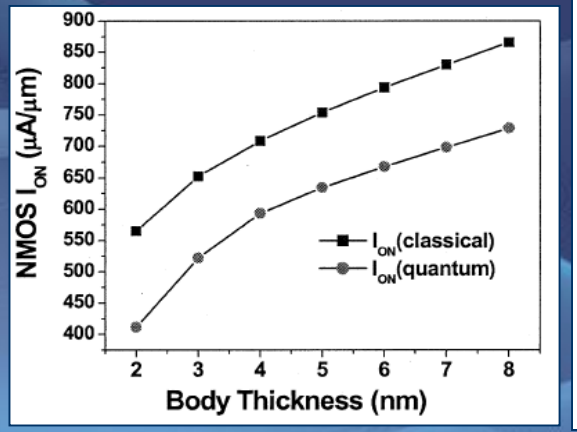
UC Berkeley Results – FinFET/ Double Gate (2000-04)

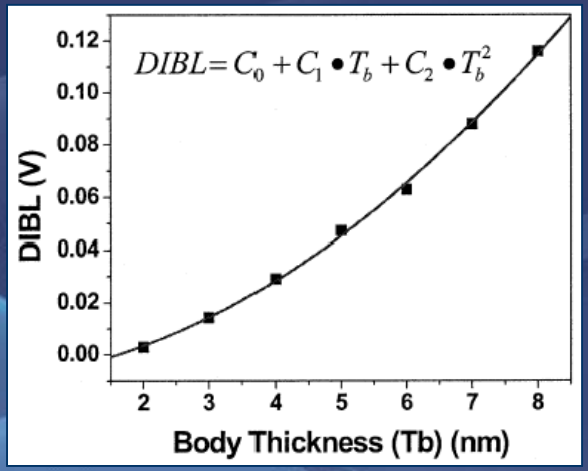


Gate Length = 30nm, Fin Width =20nm



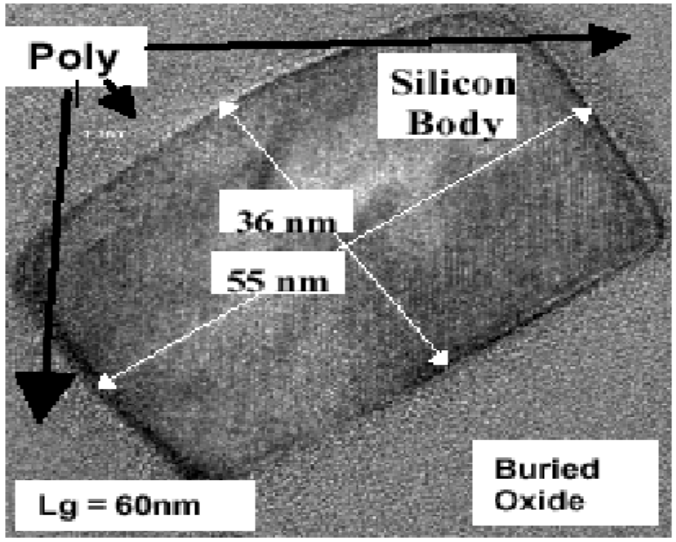
Gate Length = 30nm, Oxide thickness =2.1nm

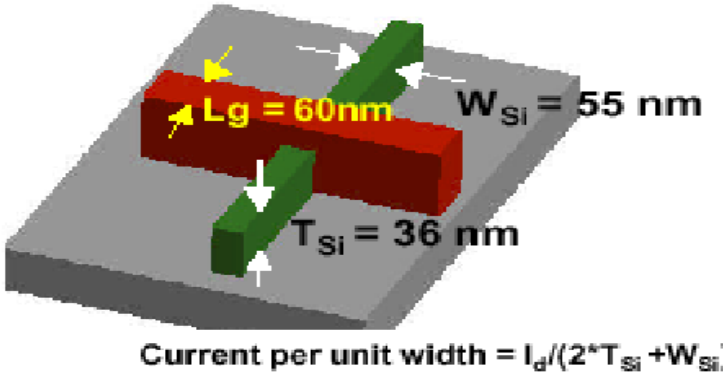




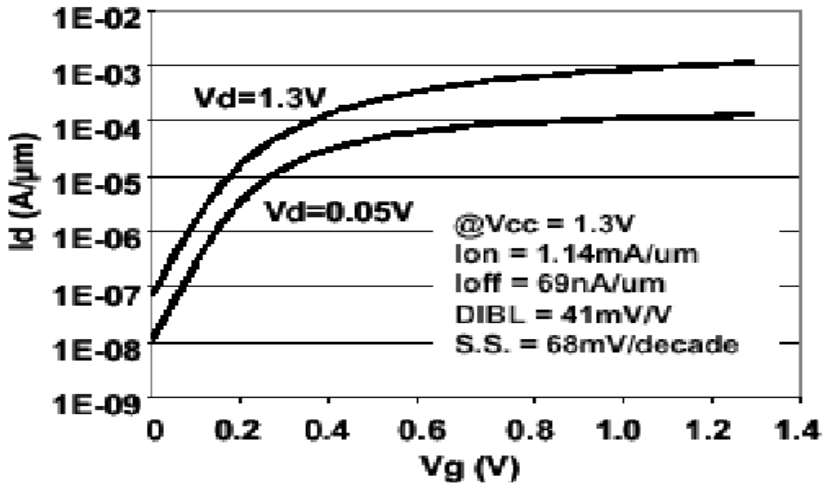
Gate Length = 20nm

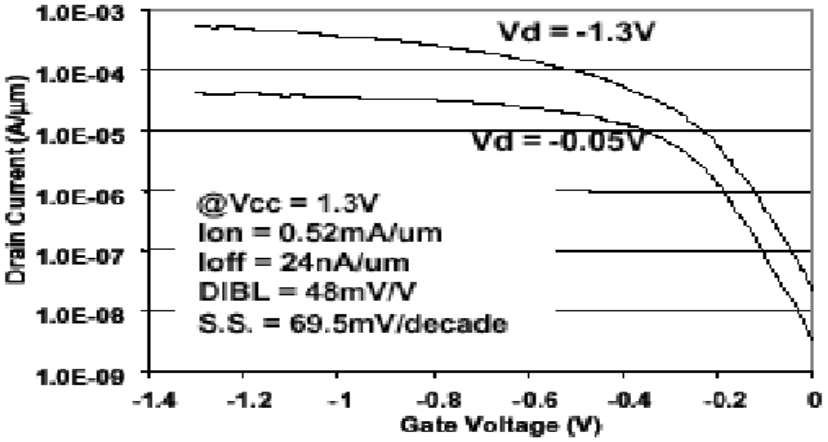
INTEL's TriGate FinFET (SSDM 2002)





Current per unit width = $I_d/(2*T_{Si}+W_{Si})$





Highest ever performance reported for NMOS and PMOS devices on a single substrate !!

TSMC's Ω-gate FINFET (SSDM-2002)

TSMC's Ω-gate (IEDM'02)