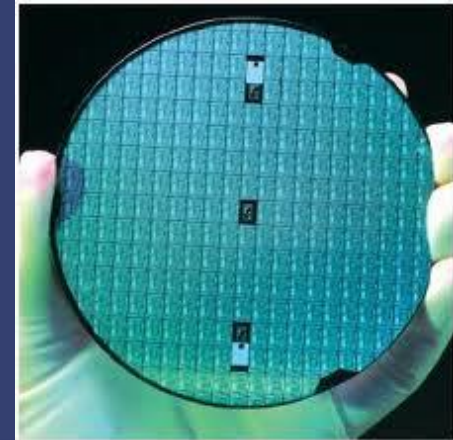
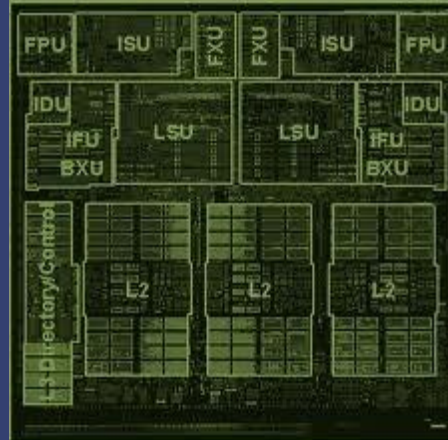
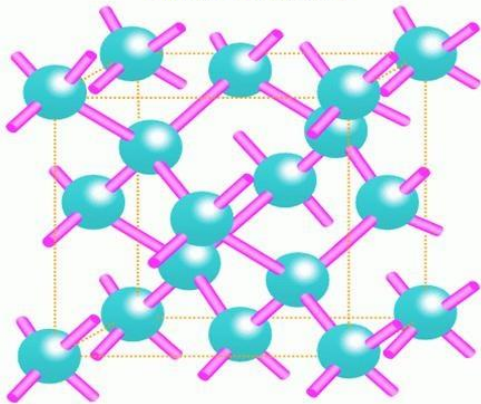


Structure of silicon crystal



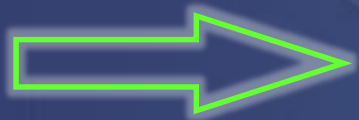
ECE 225

Lecture 6

Steep Subthreshold Slope Devices: Tunneling Field-Effect-Transistors

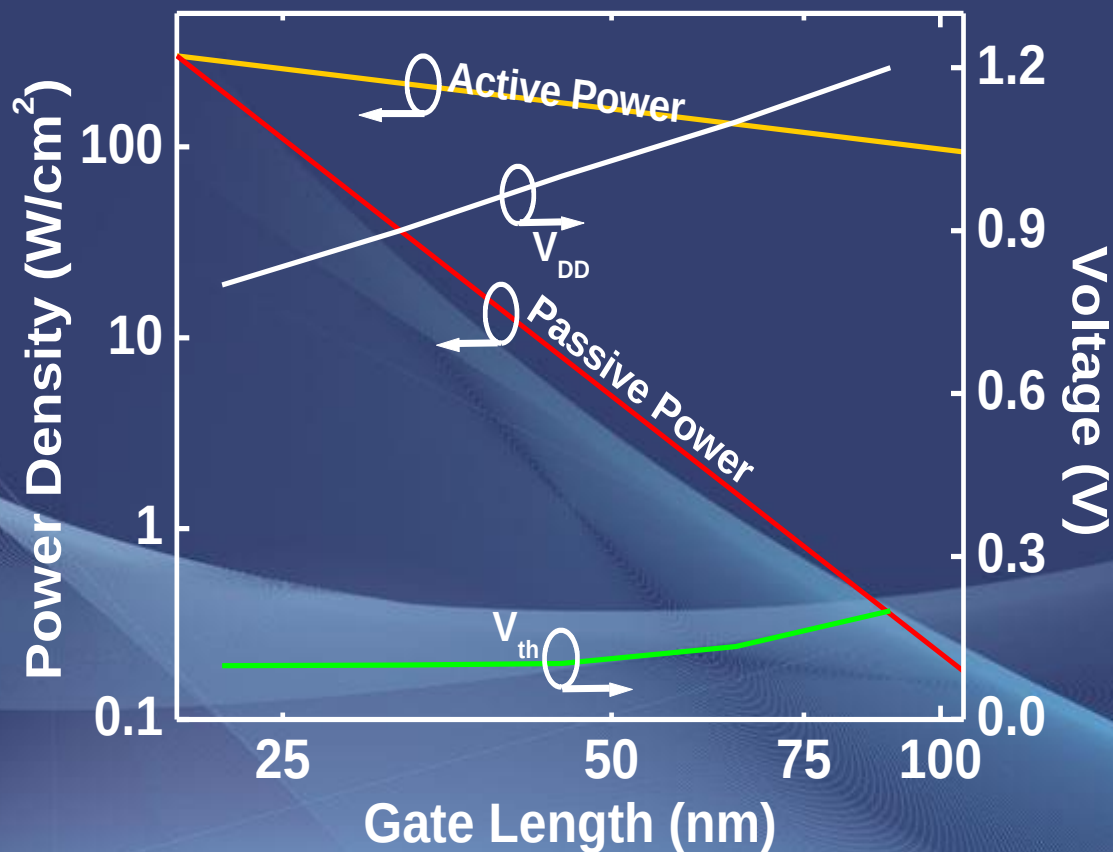
Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

Why steep sub-threshold slope (SSS) device ?



**To save power
@ the same
performance (speed)**

Power Consumption in MOSFETs



Active power $\propto C * V_{DD}^2 * f$

C :

V_{DD} :

f :

Scaling trend...

Passive power $\propto I_{OFF} * V_{DD}$

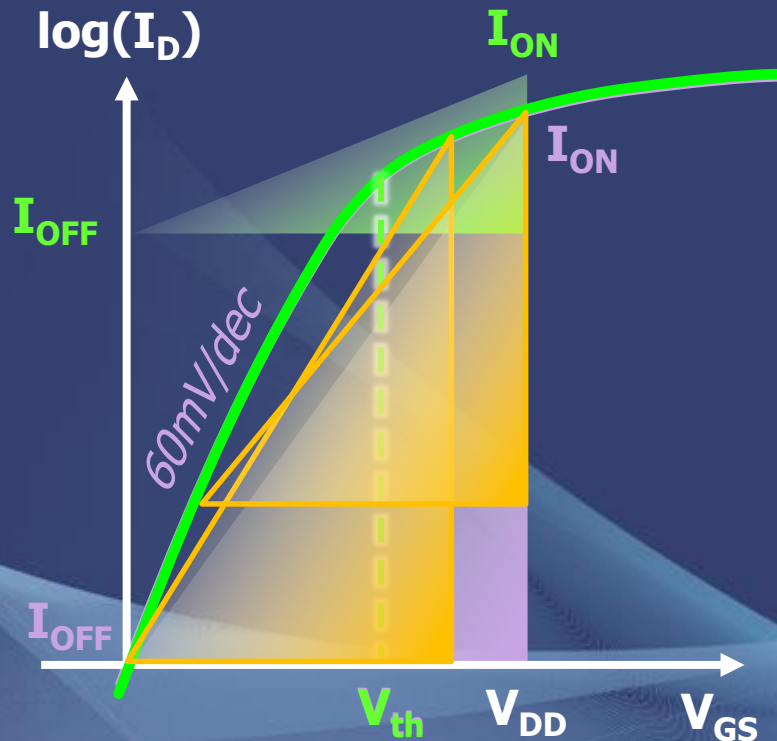
I_{OFF} :

V_{DD} :

Puri et. al., Nano Lett., 2003

The focus: V_{DD} & I_{OFF}

Power vs. Performance



Design at certain node (fixed V_{DD}):

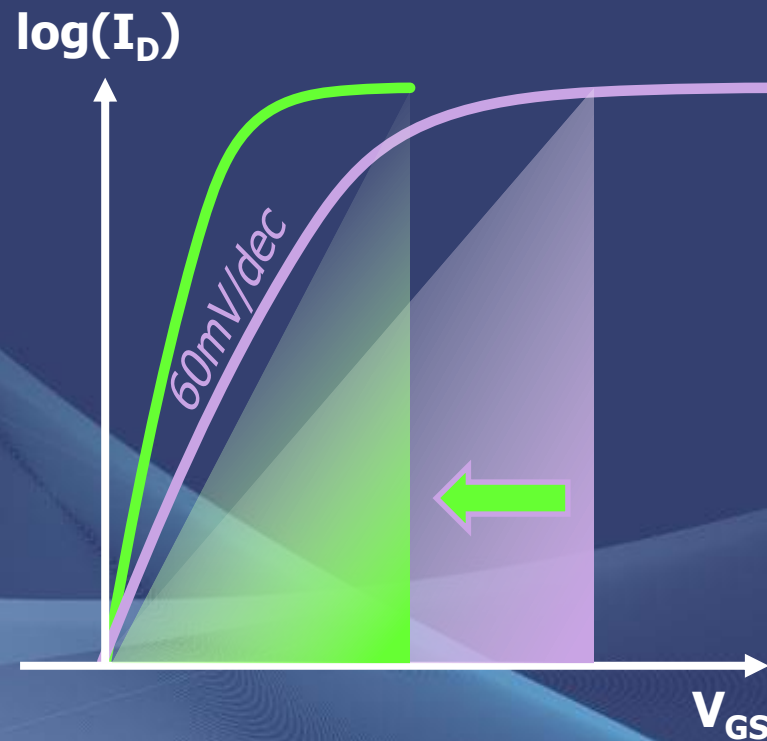
- high $V_{th} \Rightarrow$ low I_{OFF} & low I_{ON}
 $\Rightarrow$ low passive power & low performance
(low-standby-power, or LSTP)
- Low $V_{th} \Rightarrow$ high I_{OFF} & high I_{ON}
 $\Rightarrow$ high passive power & high performance
(high performance, or HP)

For V_{DD} scaling:

- ❖ At fixed I_{OFF} , smaller V_{DD} means lower I_{ON} and thus lower performance (speed)
- ❖ At fixed I_{ON} , smaller V_{DD} means higher I_{OFF} and thus higher passive power

**Power or Performance ?
One-choice dilemma
For MOSFET**

How Can SSS Device Help?



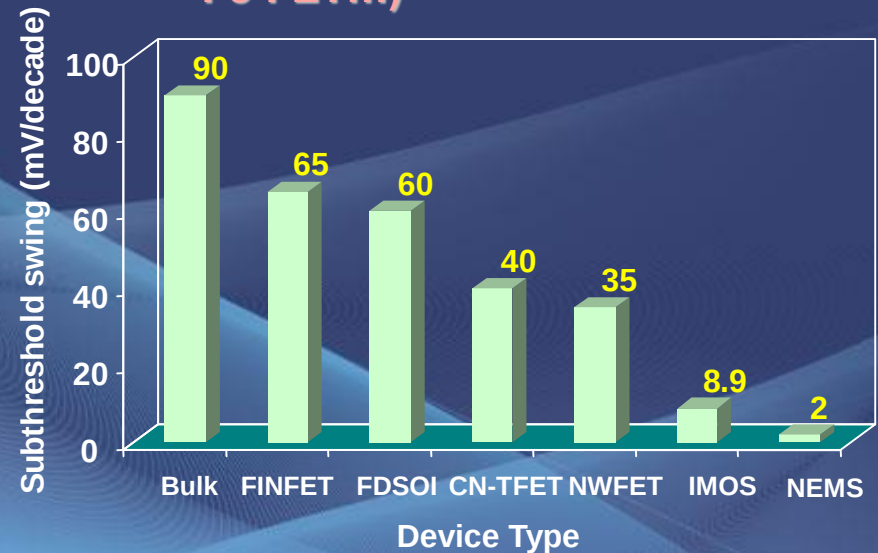
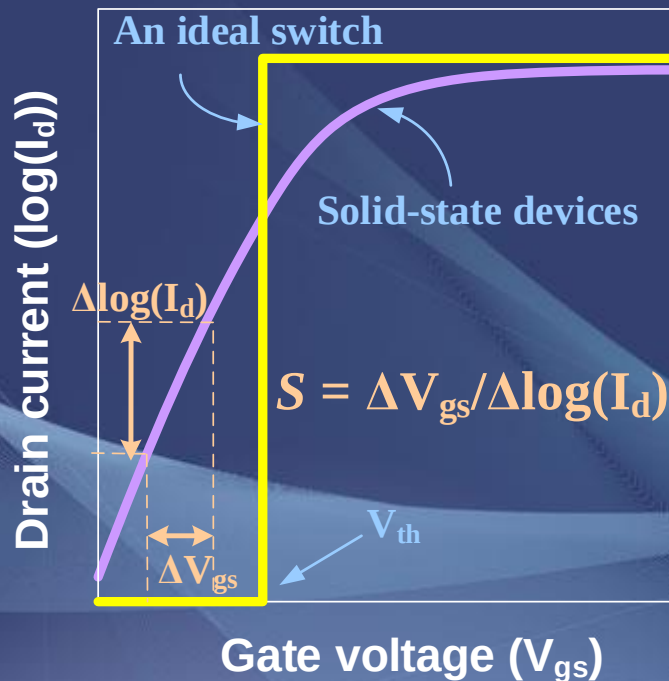
Scaling the V_{DD} , without increasing passive power, or sacrificing performance !

SSS Engineering

$$S = \underbrace{\left(\frac{d[\log I_d]}{dV_g} \right)^{-1}}_{\text{Device electrostatics limited}} = \underbrace{\frac{dV_g}{d\phi_s}}_{\text{Transport mechanism limited}} \left(\frac{1}{\ln(10) I_d} \frac{dI_d}{d\phi_s} \right)^{-1}$$

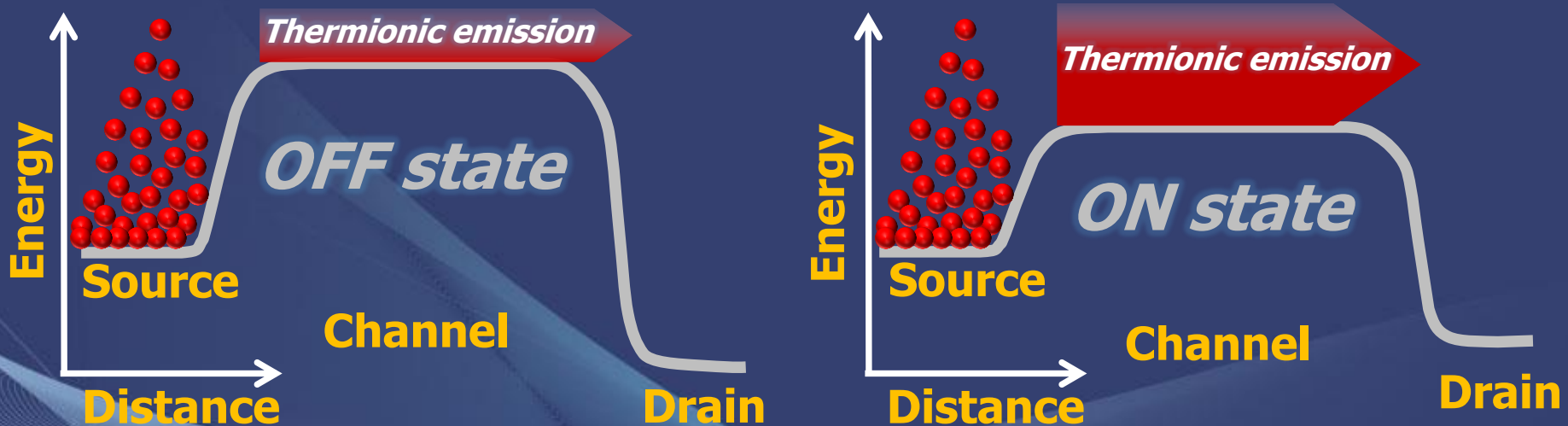
Device electrostatics limited
(NEM-FET, NWFET, Fe-FET...)

Transport mechanism limited
(TFET, IMOS...)



Dadgour et al., DAC 2007

MOSFET Carrier Transport



$$S = \left(\frac{d[\log I_d]}{dV_g} \right)^{-1} = \frac{dV_g}{d\phi_s} \left(\frac{1}{\ln(10) I_d} \frac{dI_d}{d\phi_s} \right)^{-1}$$

Depends on device
electrostatics

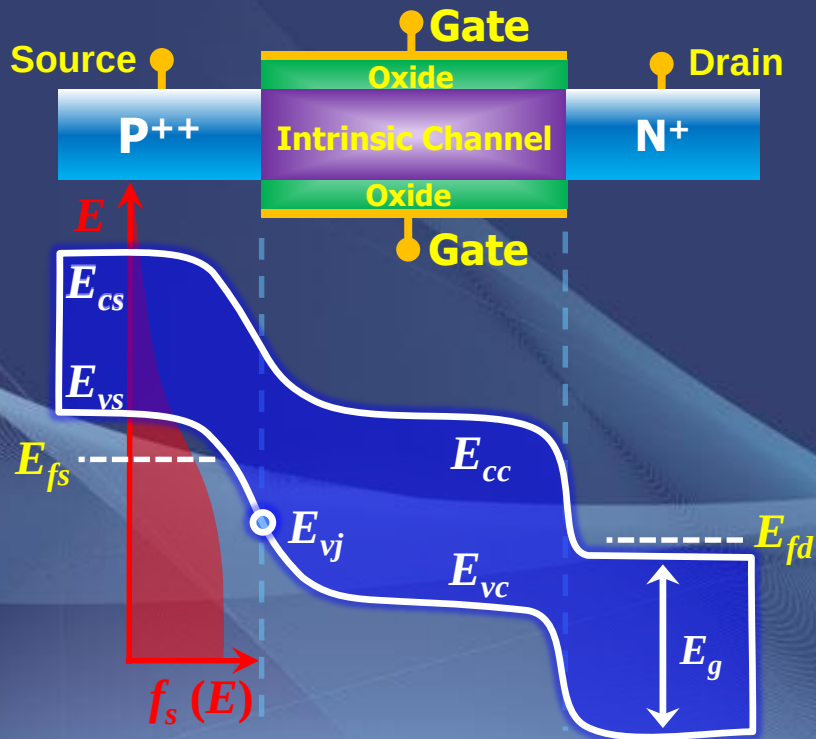
$$I_d = \text{const.} \exp\left(-\frac{q\phi_s}{kT}\right)$$

60mV/dec @ RT

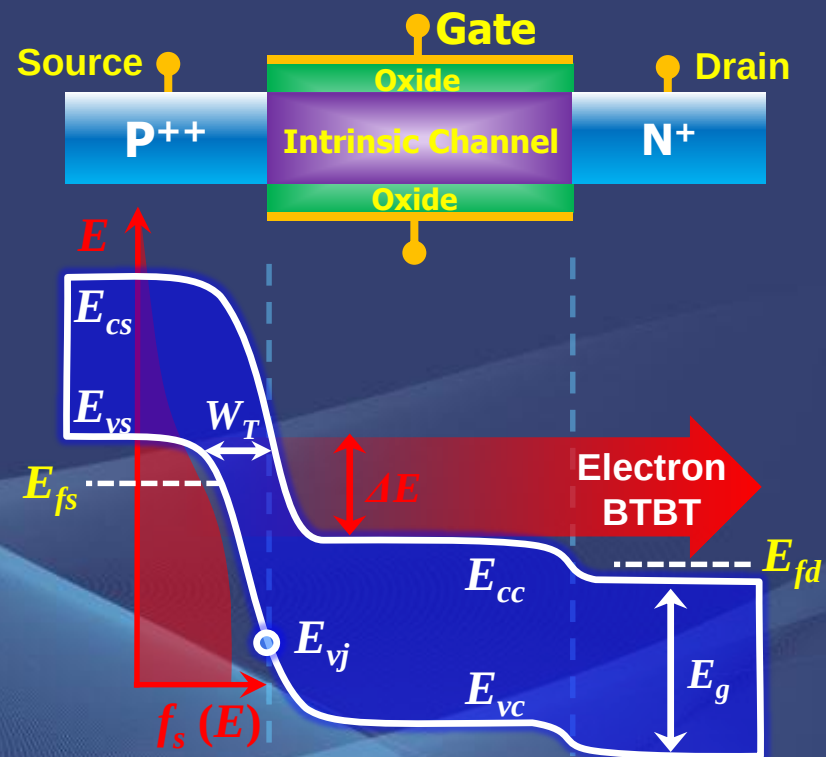
Fundamentals of Tunnel FET

--- the most promising SSS device

OFF state



ON state



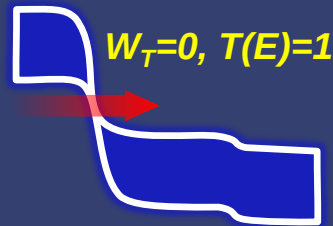
Abrupt appearance of conduction channel (tunneling window) is the key in achieving SSS!

Origin of SSS in TFET

--- from a mathematical perspective

$$I_{ds} = \frac{2q}{h} \int_{E_{cc}}^{E_{vs}} T(E) [f_s(E) - f_d(E)] dE$$

$$\approx \frac{2q}{h} F_{Integral}$$



Consider an idealized TFET

$$F_{Integral} = kT \ln \left(\frac{1 + \exp \left[(E_{fs} - E_{vs} + \Delta E) / kT \right]}{1 + \exp \left[(E_{fs} - E_{vs}) / kT \right]} \right)$$

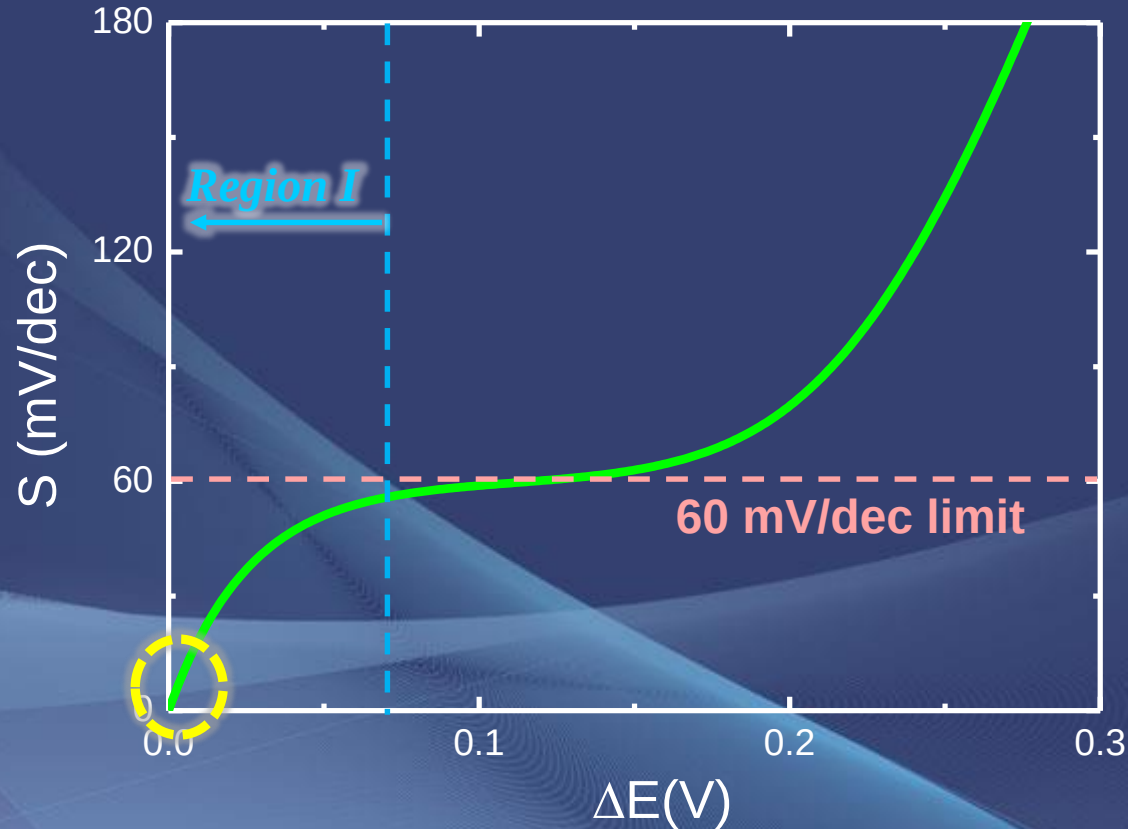
V_{ds} is large
 $\Rightarrow f_d(E) \sim 0$

$$\Delta V_g = \Delta E / q$$

$$S = \left(\frac{d \log_{10} (F_{Integral})}{d (\Delta E / q)} \right)^{-1}$$

$$= \frac{\ln(10)kT}{q} \left(1 + \exp \left(\frac{E_{vs} - E_{fs} - \Delta E}{kT} \right) \right) \ln \left(\frac{1 + \exp \left((E_{fs} - E_{vs} + \Delta E) / kT \right)}{1 + \exp \left((E_{fs} - E_{vs}) / kT \right)} \right)$$

Near-zero S in TFET



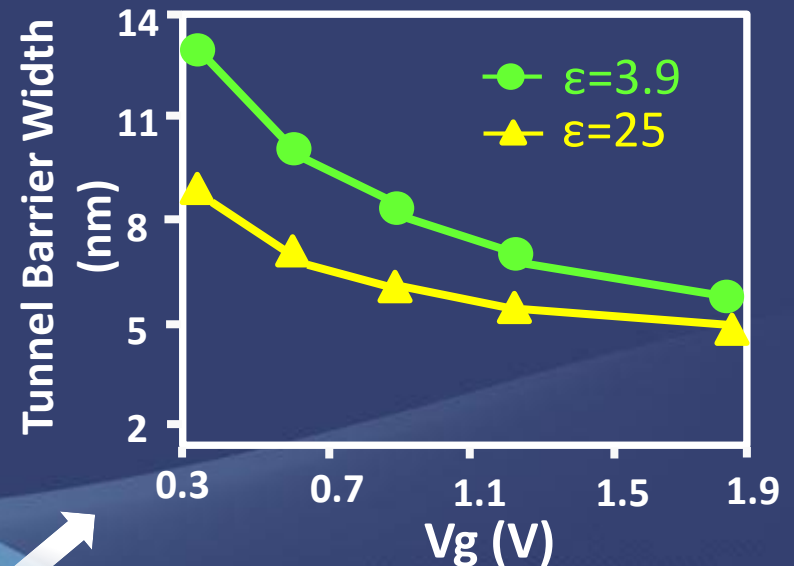
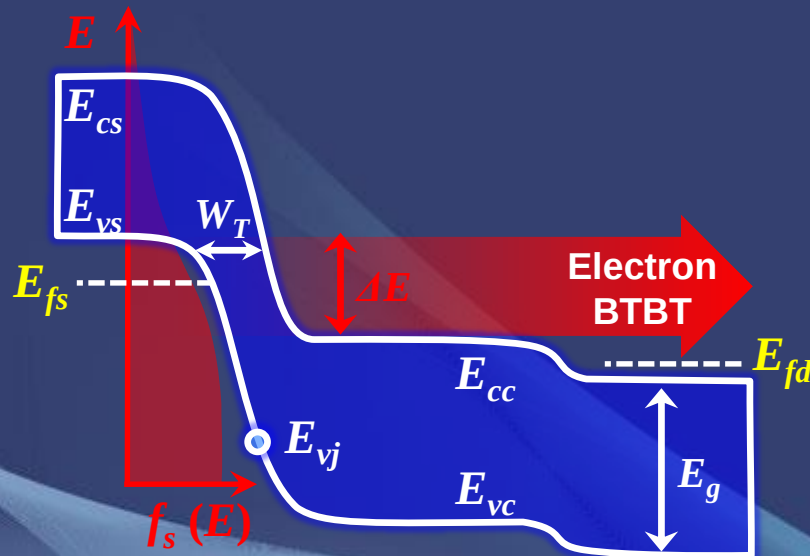
$$SS \xrightarrow{\text{region I}} \ln(10) \frac{kT}{q} \left(1 - \exp\left(\frac{-\Delta E}{kT}\right) \right)$$

Large $\Delta E \rightarrow \ln(10) \frac{kT}{q}$

Small $\Delta E \rightarrow 0$

The Limitations of TFET

1. Low ON current



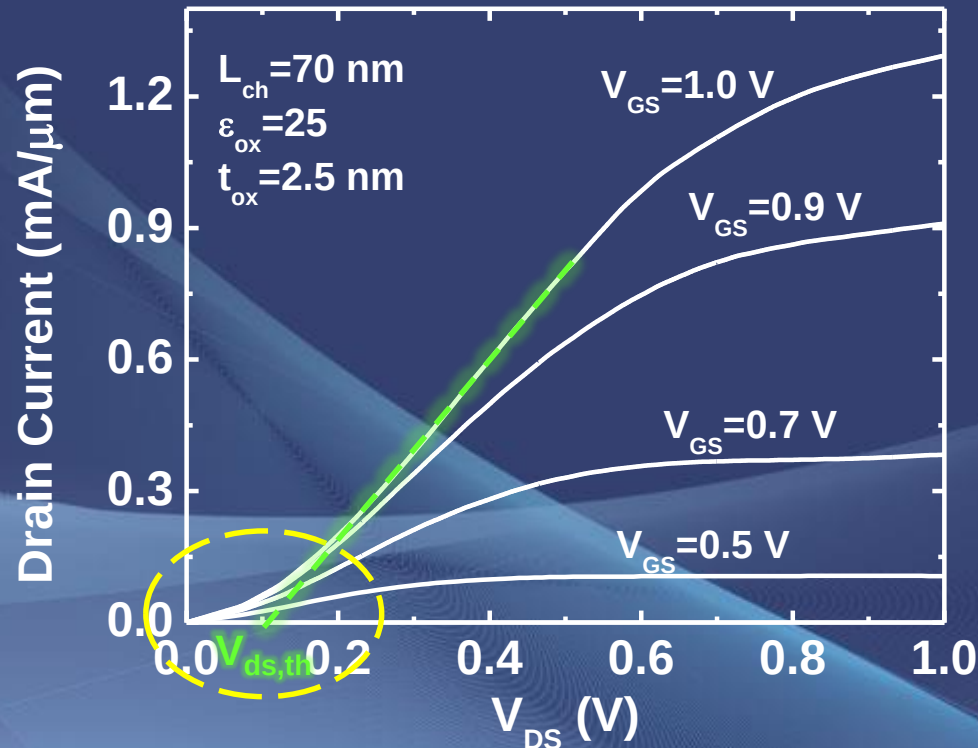
K. Boucart et al., TED 2007.

$W_T \neq 0$ (~Several nanometers)

$$T(E) \approx \exp\left(-\frac{4W_T \sqrt{2m^*} E_g^{3/2}}{3|e|\hbar(\Delta E + E_g)}\right) \ll 1$$

The Limitations of TFET

2. Slow V_{ds} turn-on

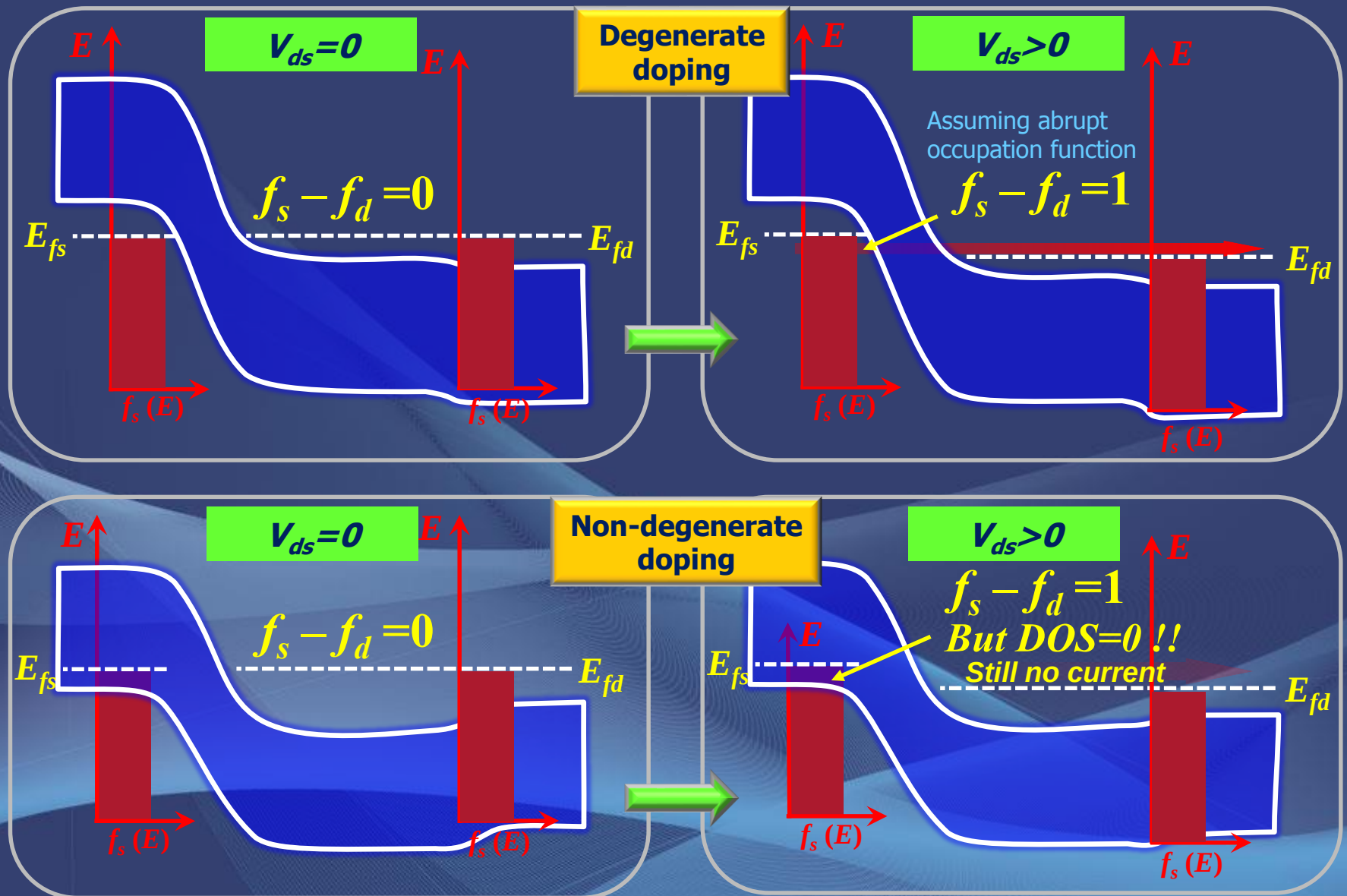


Why?

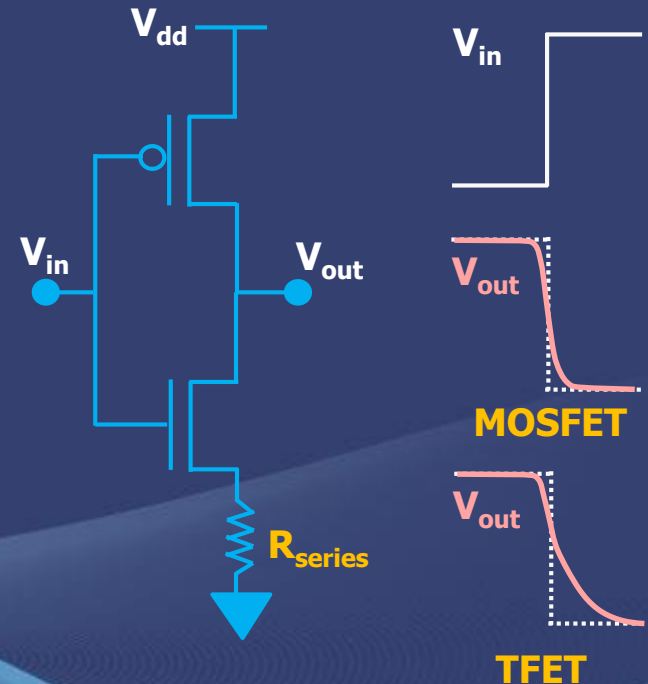
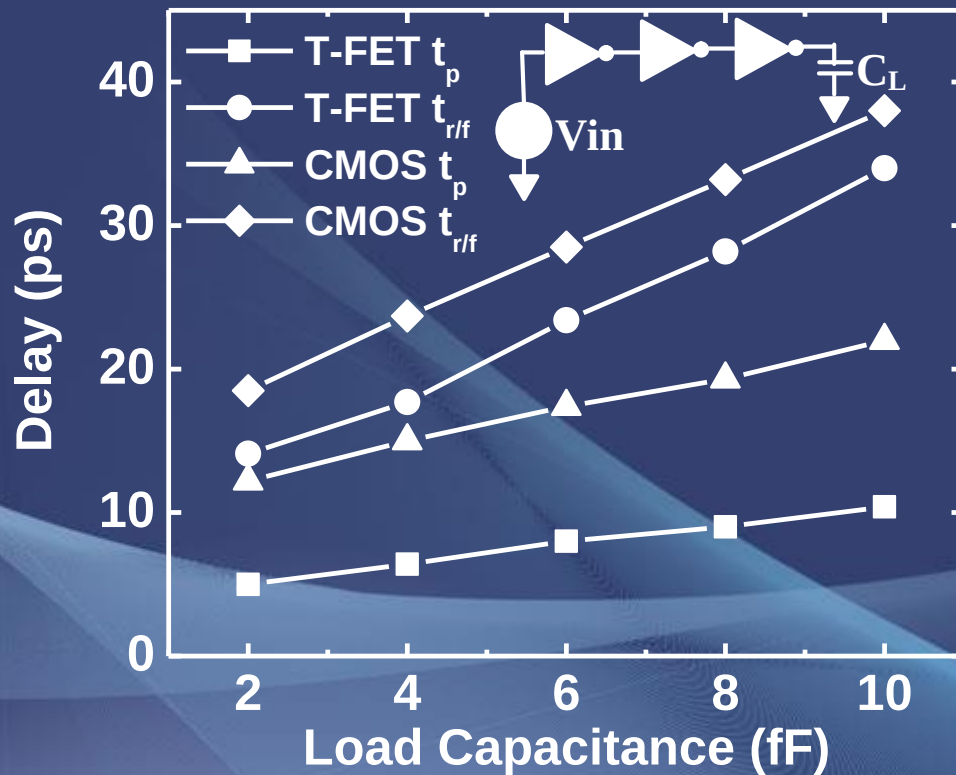
Any effect on circuit performance ?

Origin of $V_{ds,th}$ in TFET

--- from a physics perspective



Effect on Circuit

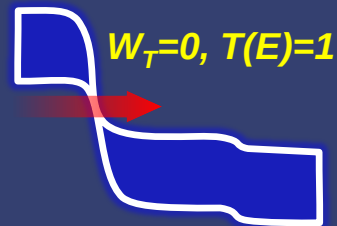


Origin of $V_{ds,th}$ in TFET

--- from a mathematical perspective

$$I_{ds} = \frac{2q}{h} \int_{E_{cc}}^{E_{vs}} T(E) [f_s(E) - f_d(E)] dE$$

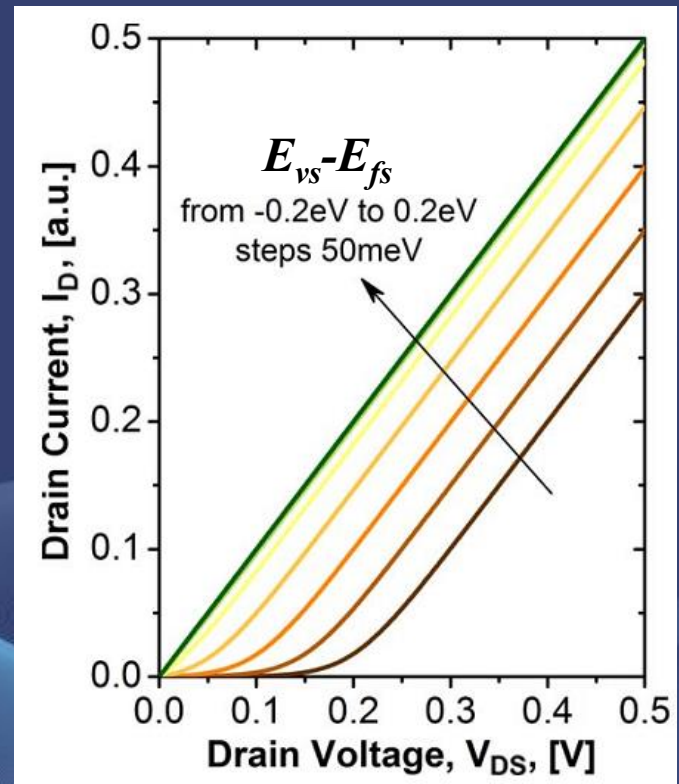
$$\approx \frac{2q}{h} F_{Integral}$$



$$F_{Integral} = kT \ln \left(\frac{1 + \exp \left[(E_{fs} - E_{vs} + \Delta E) / kT \right]}{1 + \exp \left[(E_{fs} - E_{vs}) / kT \right]} \right) - kT \ln \left(\frac{1 + \exp \left[(E_{fd} - E_{vs} + \Delta E) / kT \right]}{1 + \exp \left[(E_{fd} - E_{vs}) / kT \right]} \right)$$

$$E_{fs} - E_{fd} = qV_{ds}$$

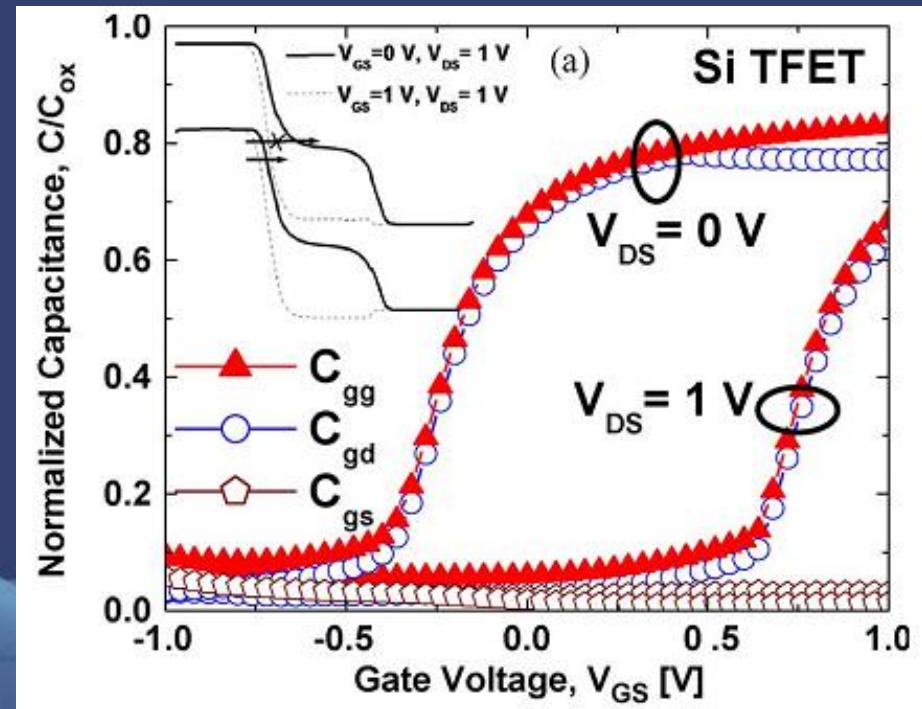
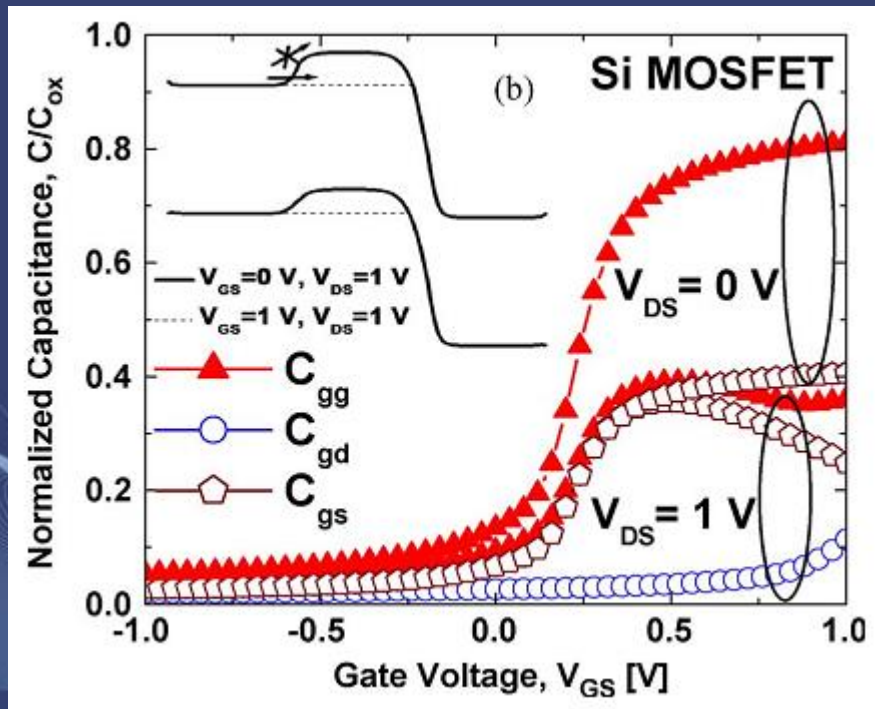
Consider an idealized TFET



Degenerate doping is needed in the source to eliminate $V_{ds,th}$

The Limitations of TFET

3. Large C_{gd}



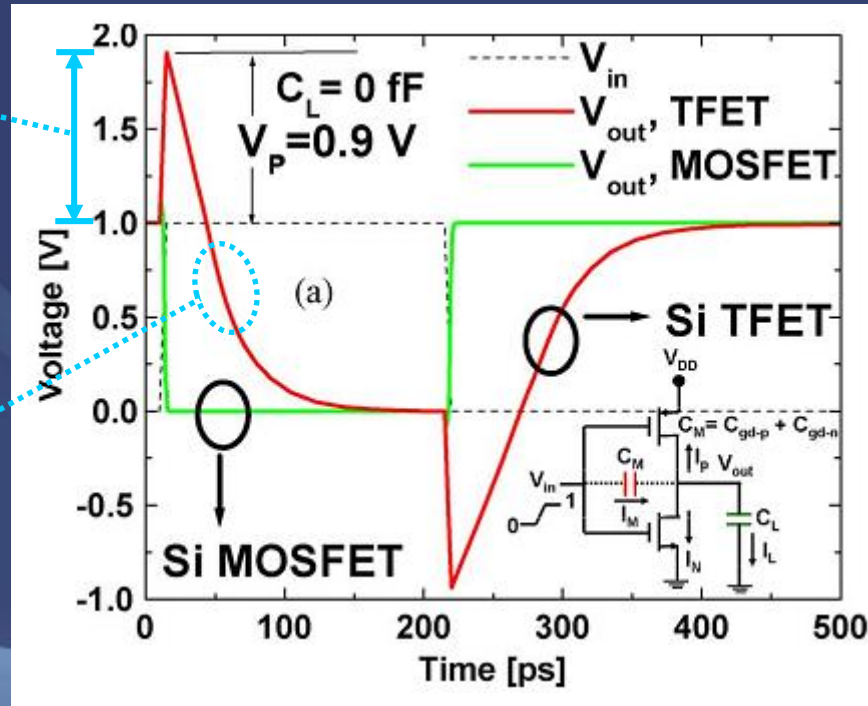
In MOSFET, C_{gs} and C_{gd} evenly divide C_{gg} in linear region; C_{gs} dominates in saturation regions

In TFET, C_{gd} dominates in both linear and saturation regions

Enhanced Miller Effect

Depends
on C_M

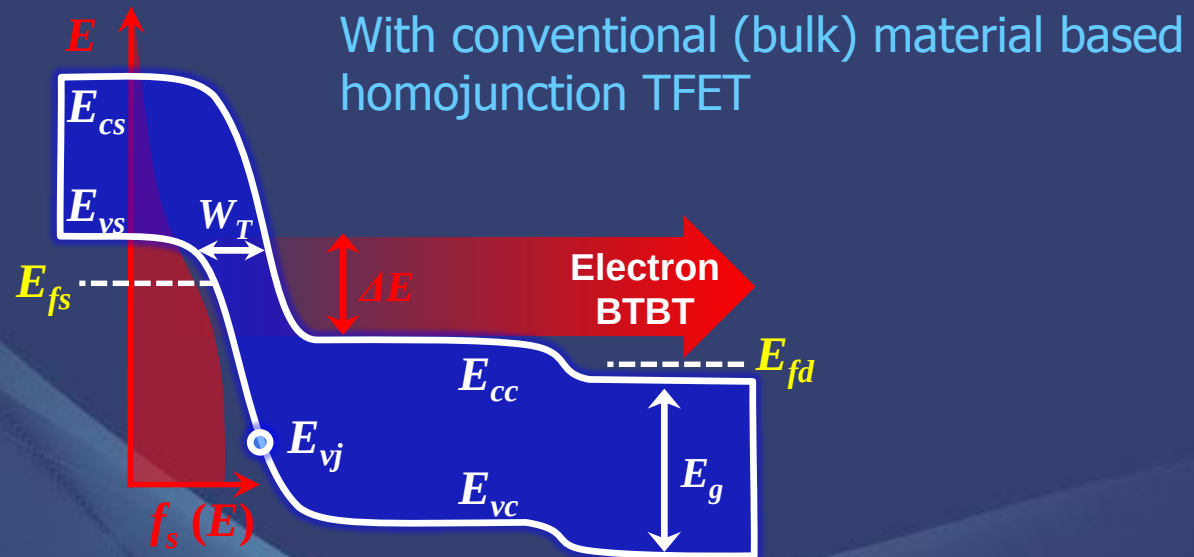
$V_{ds,th}$
contributes



MILLER CAPACITANCE $C_M = C_{gd,n} + C_{gd,p}$ FOR Si TFET/MOSFET INVERTER FOR VARIOUS POINTS ALONG THE DC TRANSFER CHARACTERISTICS, AS SHOWN IN FIG. 3(b). HERE, $C_{gg} = 0.8 C_{ox}$

	A	B	C	D	E
MOSFET	$0.5C_{gg} + 0.03C_{gg}$ (p-lin, n-cutoff)	$0.5C_{gg} + 0.04C_{gg}$ (p-lin, n-sat)	$0.2C_{gg}$ (p-sat, n-sat)	$0.5C_{gg} + 0.04C_{gg}$ (p-sat, n-lin)	$0.5C_{gg} + 0.03C_{gg}$ (p-cutoff, n-lin)
TFET	$C_{gg} + 0.05C_{gg}$ (p-lin, n-cutoff)	$C_{gg} + 0.08C_{gg}$ (p-lin, n-sat)	$1.1C_{gg}$ (p-sat, n-sat)	$C_{gg} + 0.08C_{gg}$ (p-sat, n-lin)	$C_{gg} + 0.05C_{gg}$ (p-cutoff, n-lin)

TFET Design



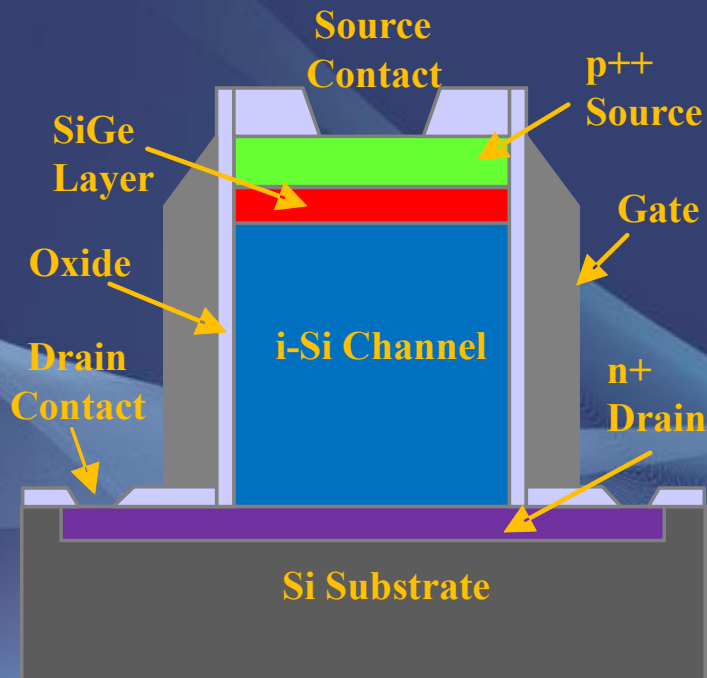
$$T(E) \approx \exp\left(-\frac{4W_T\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(\Delta E + E_g)}\right)$$

Device Structure
(W_T)

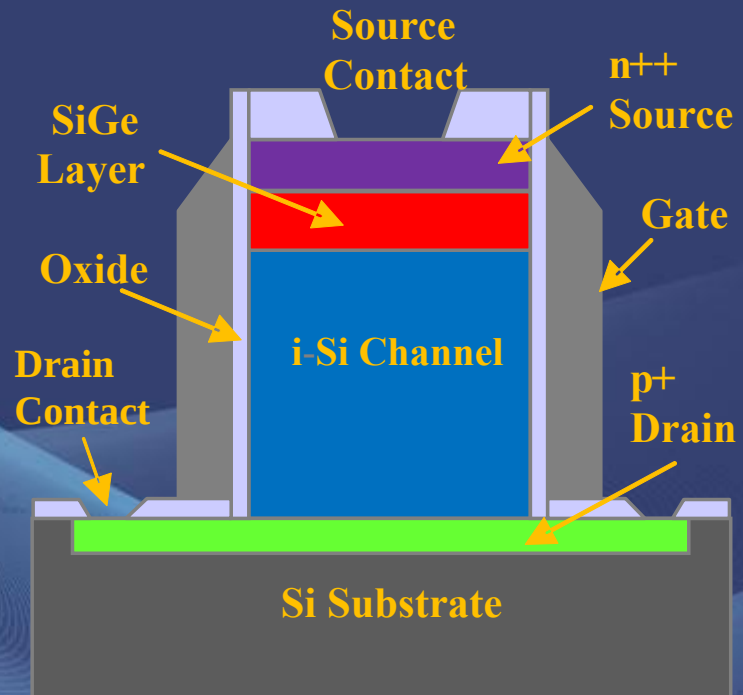
Channel Material
(m^*, E_g)

Heterojunction TFET

n-TFET



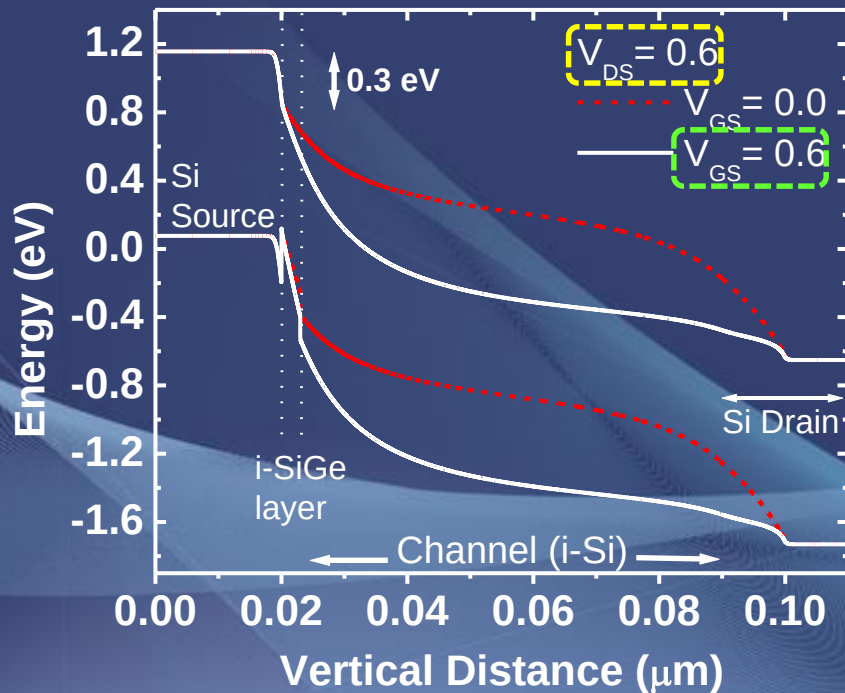
p-TFET



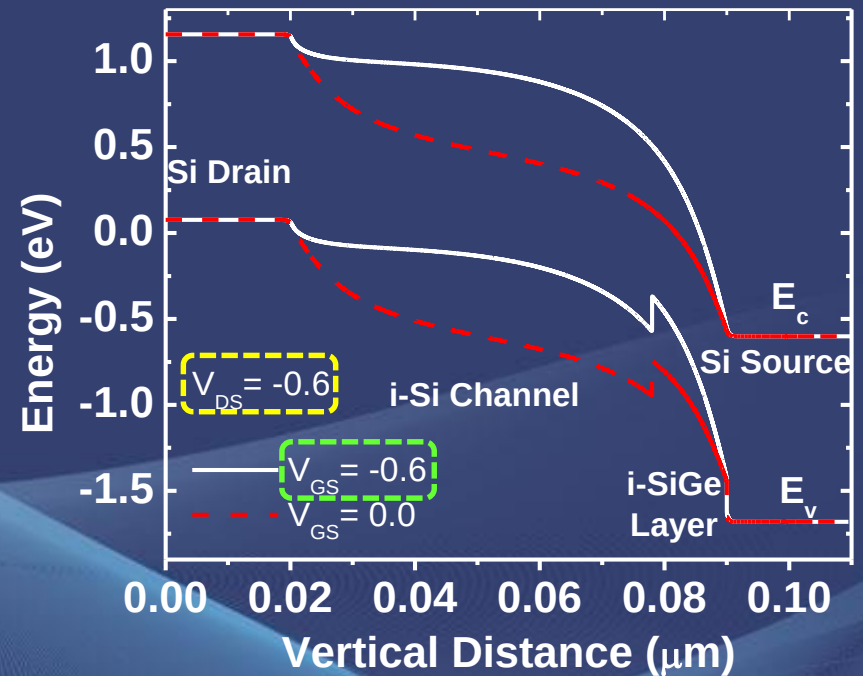
Gate electric field is perpendicular to transport direction....

Band diagram

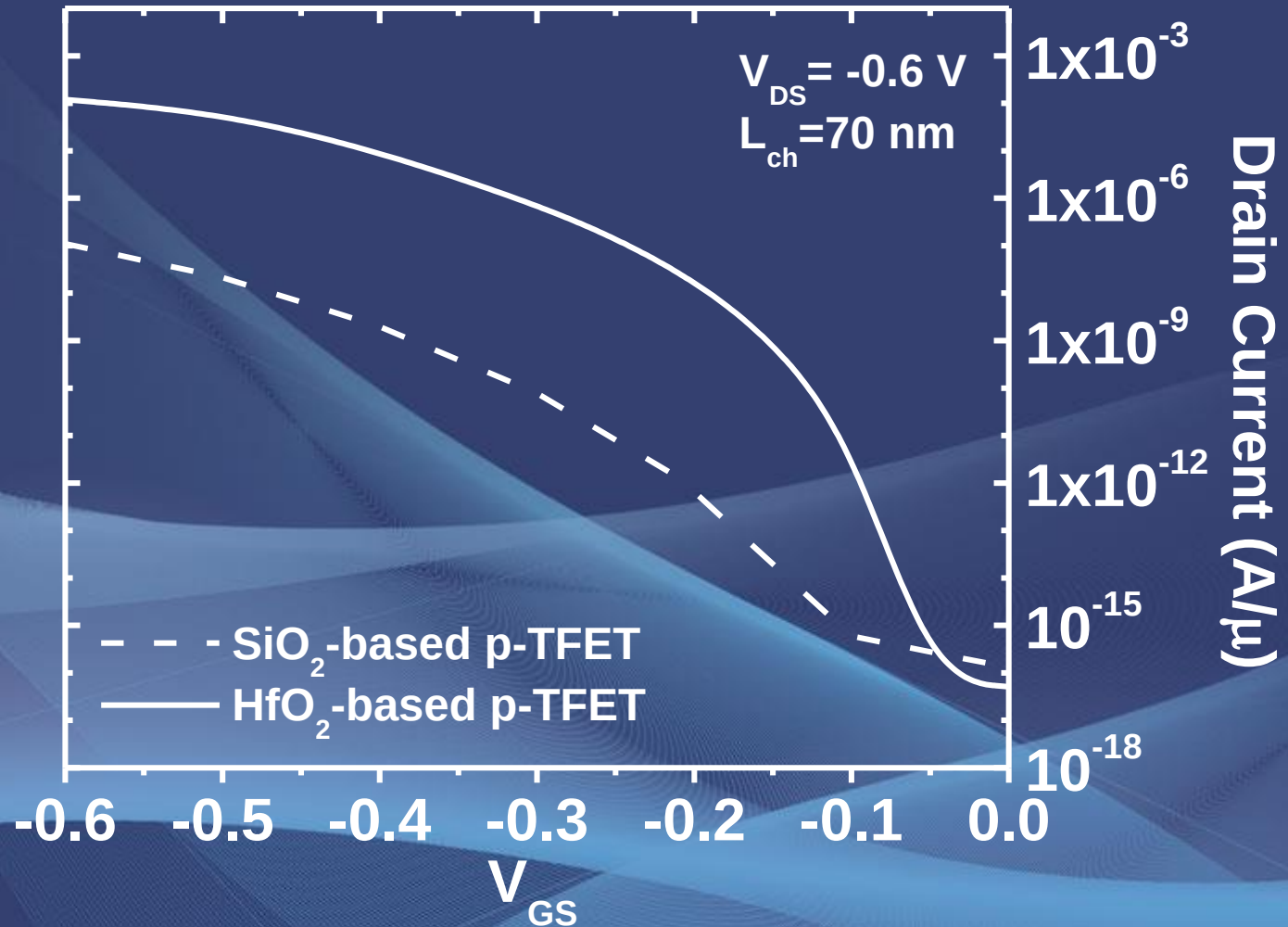
(n-TFET)



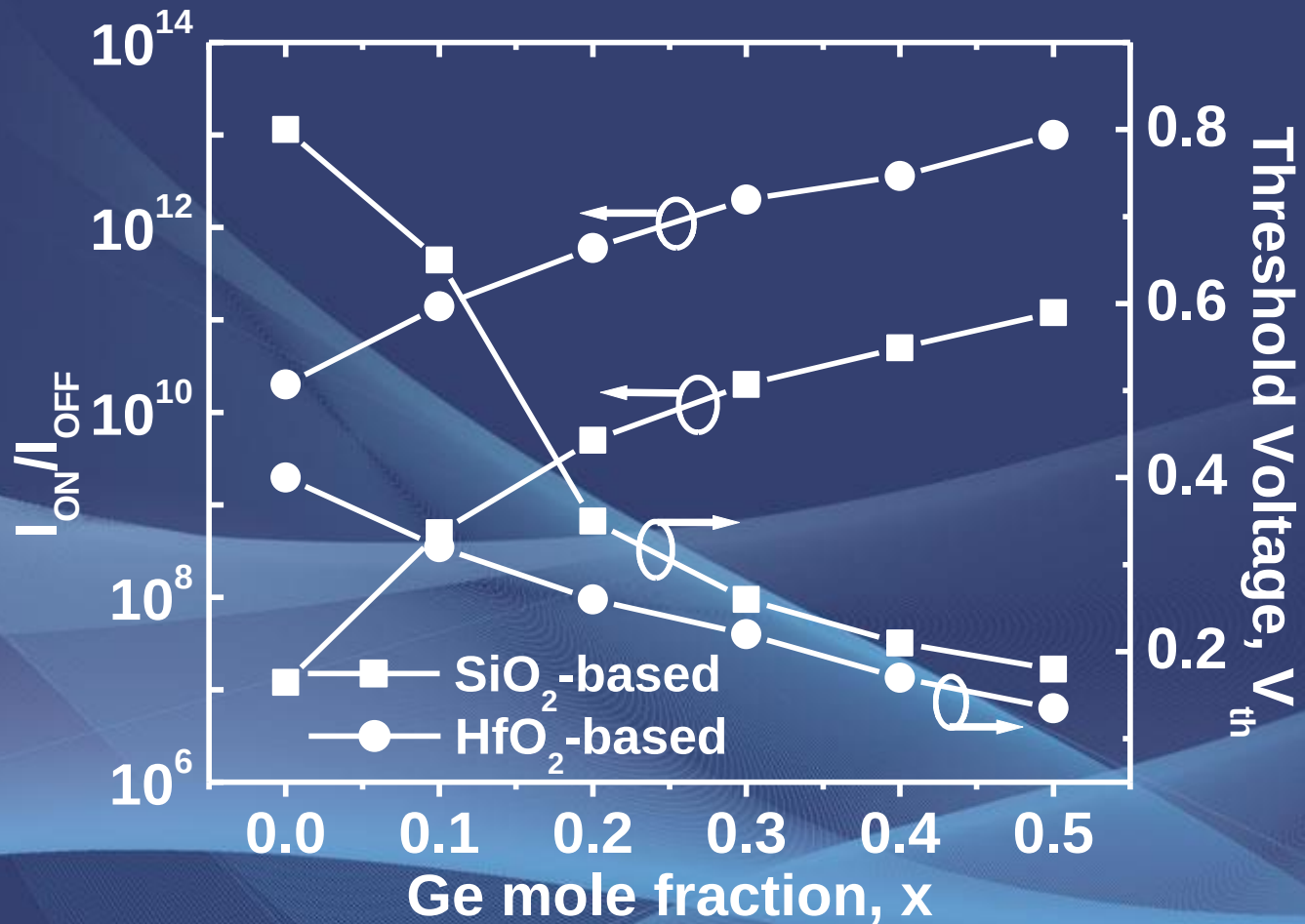
(p-TFET)



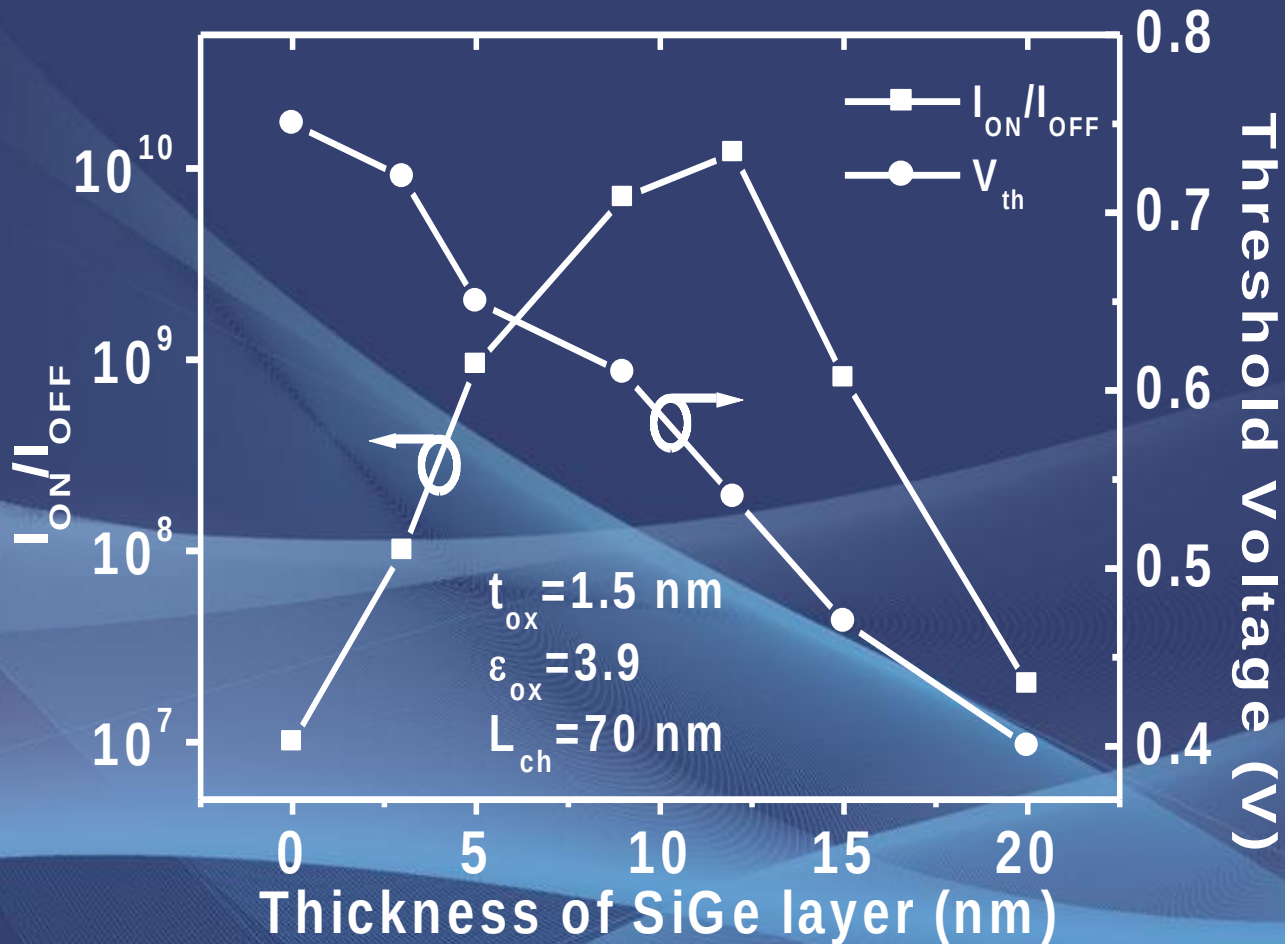
Using High-K gate dielectric



Optimizing Ge mole fraction

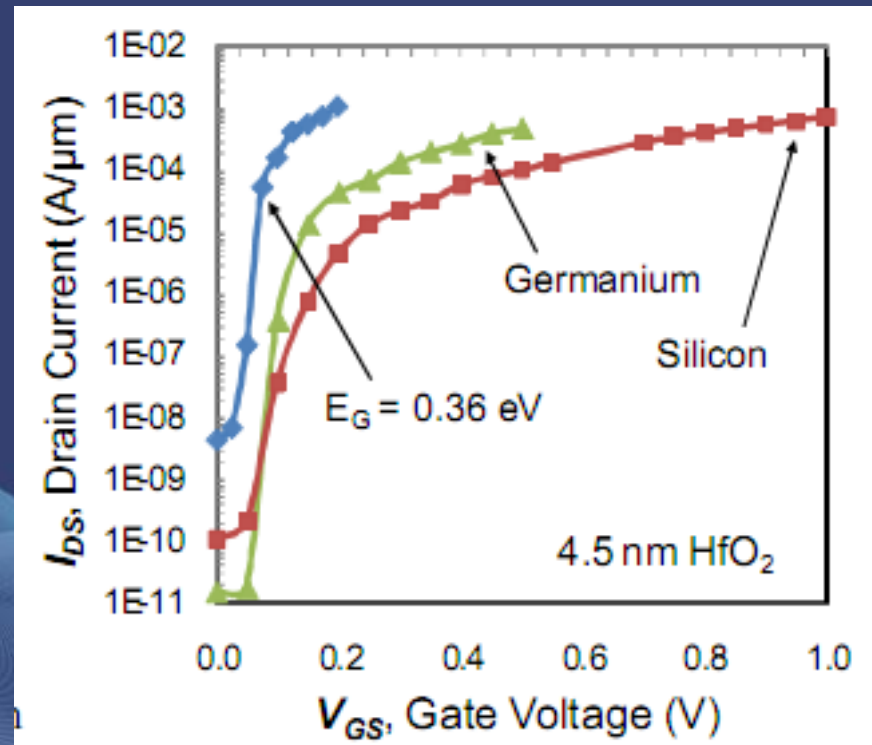
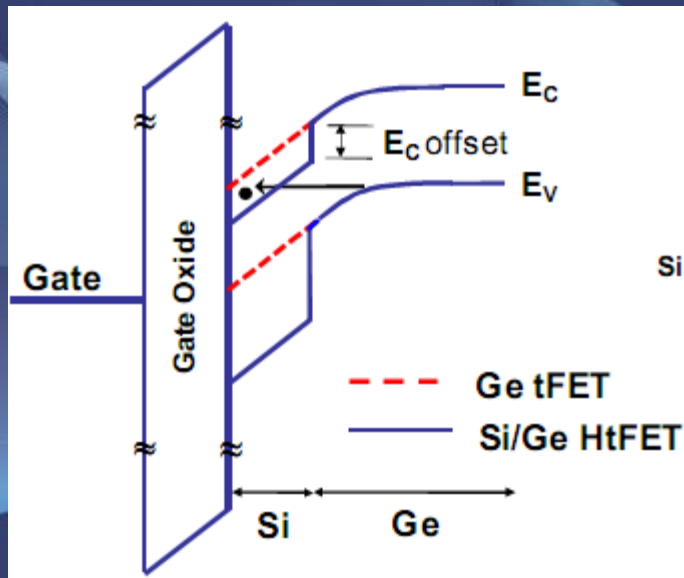
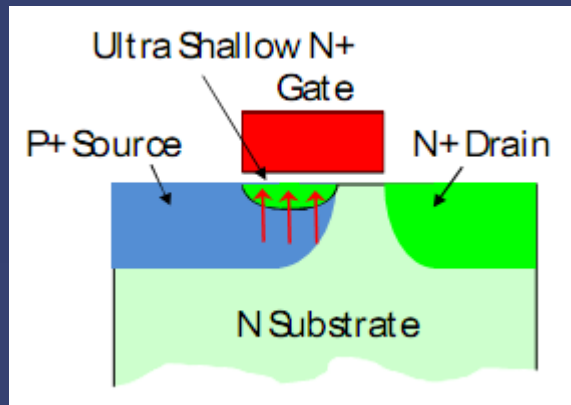


Optimizing SiGe thickness



Green FET

Gate electric field is parallel to transport direction....



Hu et al., IEDM 2010 (Berkeley)

Si Nanowire TFET

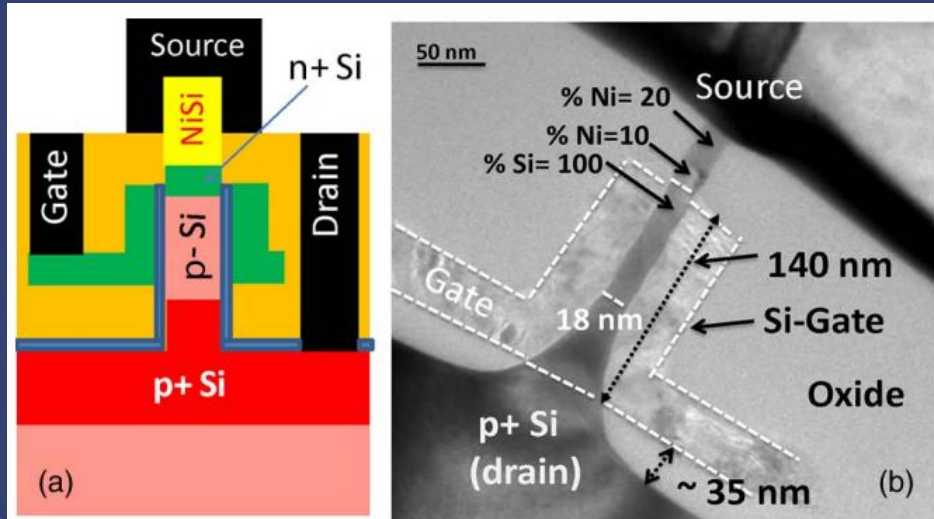
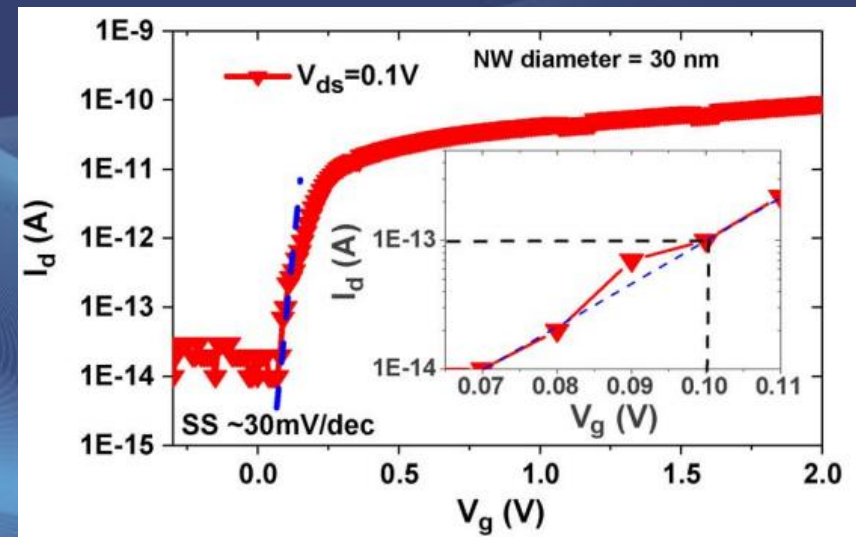
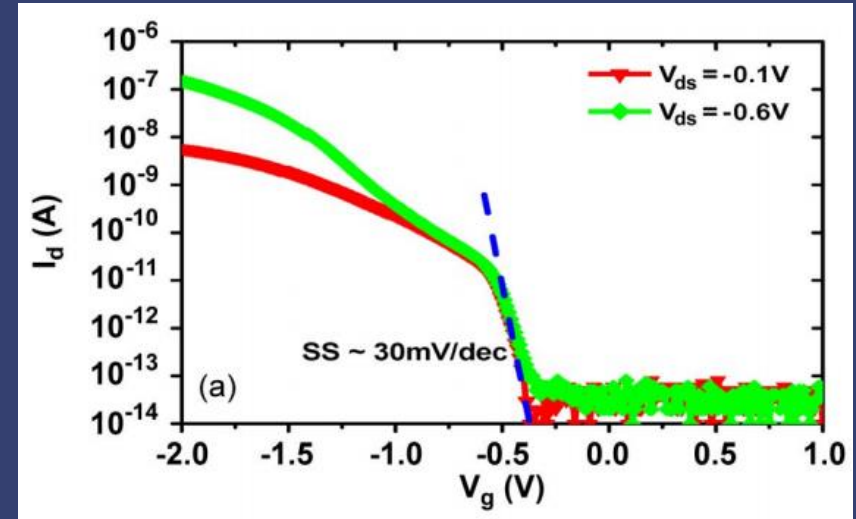
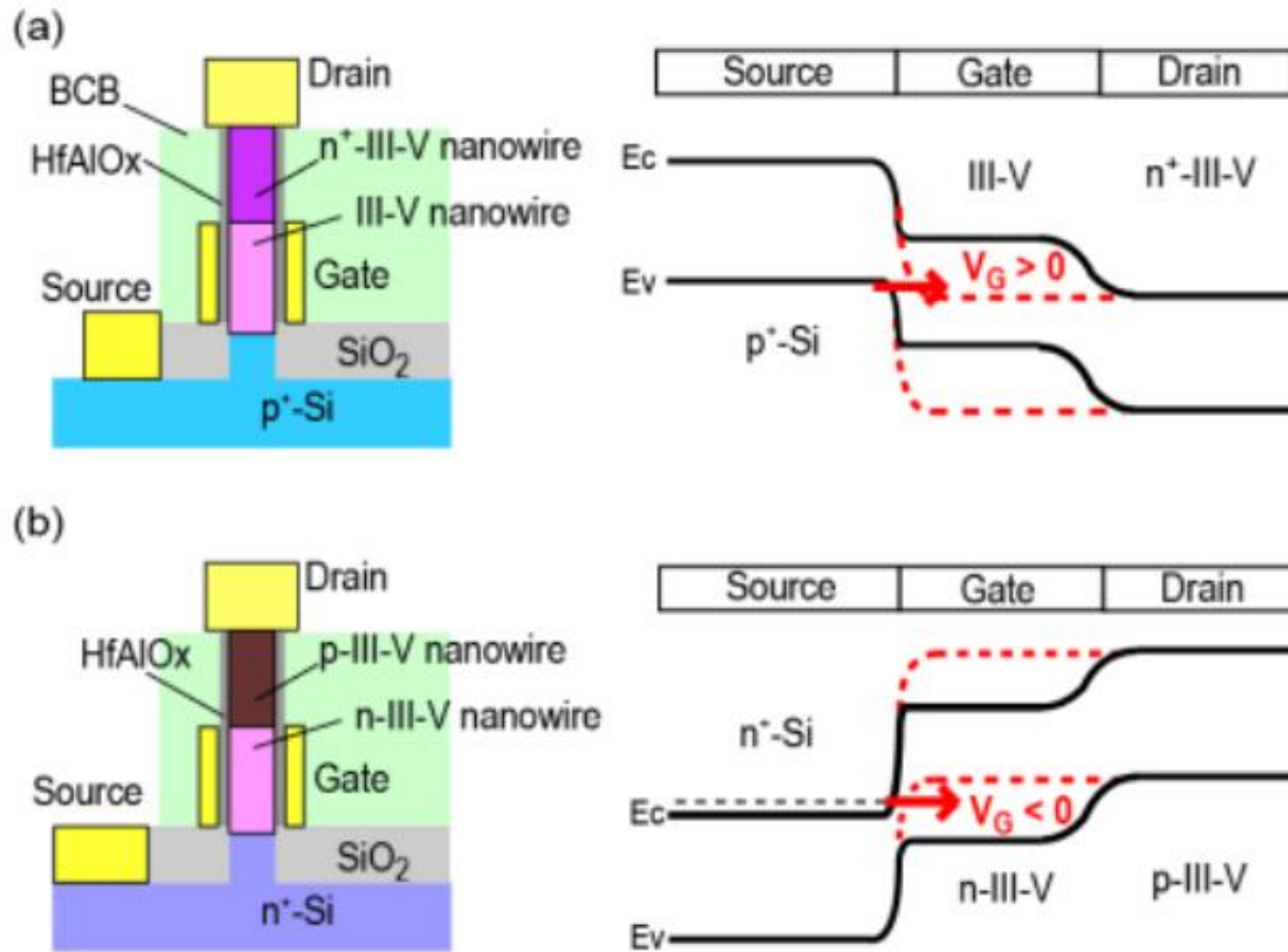


Fig. 1. (a) Device schematic and (b) TEM image of the fabricated device with a nanowire diameter of ~ 18 nm and a gate length of ~ 140 nm.



R. Gandhi et al, vol. 32, no. 4, pp. 437-439, EDL 2011

III-V-Si hetero-J TFET



III-V-Si hetero-J TFET

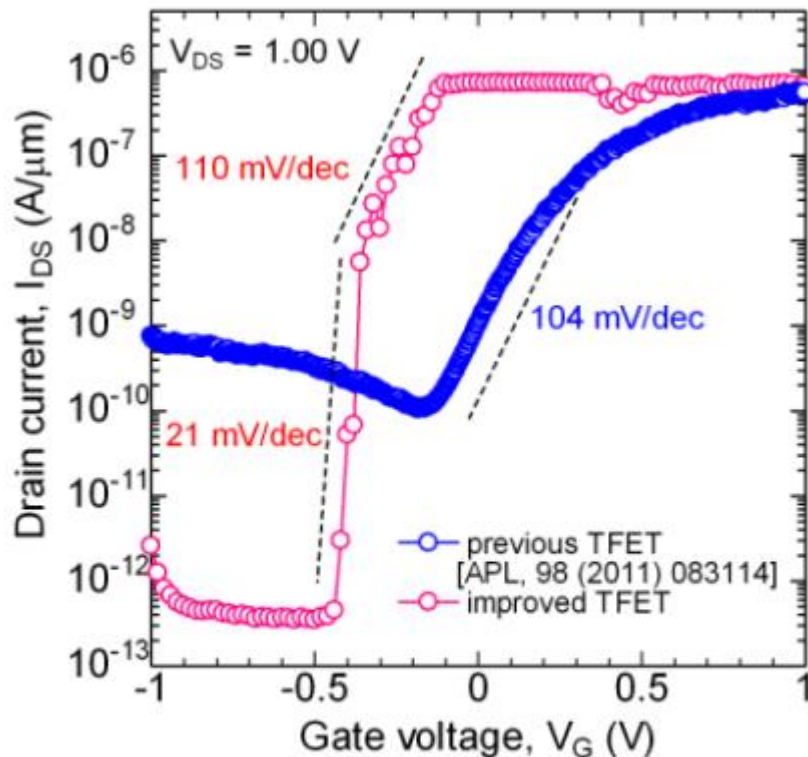


Fig. 9 Experimental transfer characteristics of optimized TFET with a NW-diameter of 30 nm (pink curve) $V_{DS} = 1.00$ V.

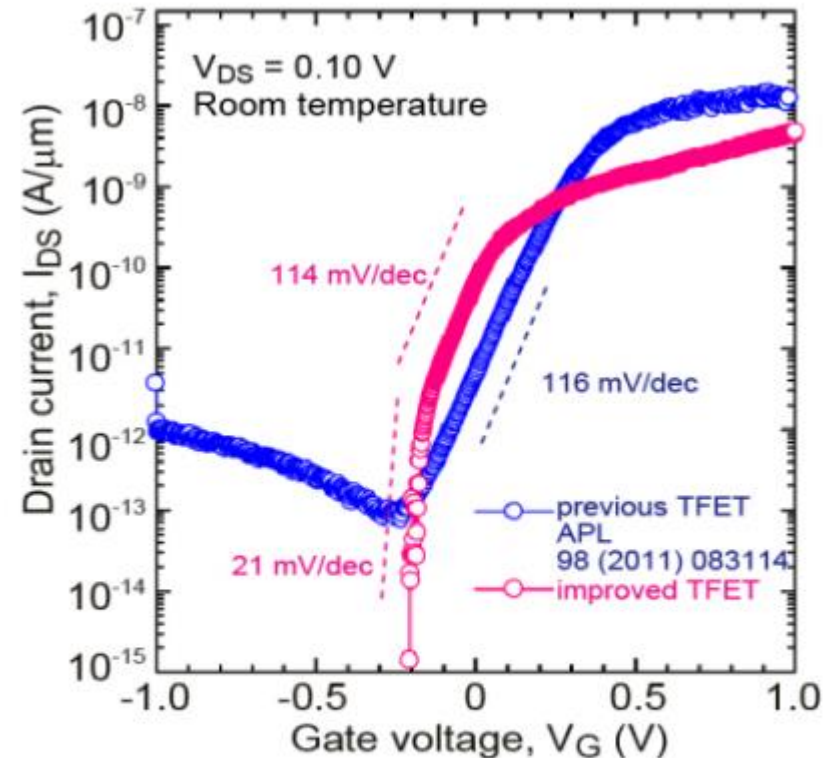


Fig. 10 Experimental transfer characteristics of optimized TFET with a NW-diameter of 30 nm (pink curve) $V_{DS} = 0.10$ V.

TFET Challenges with Bulk Materials...



- Large tunnel barrier height and width
- High density of traps near the junction

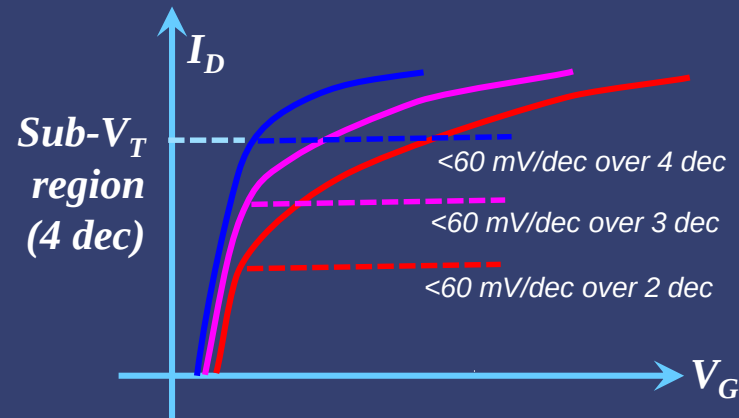
- Poor SS and I_{ON}



TFETs Designed with Bulk Materials...



requires < 60 mV/dec
over 4 decades of drain
current



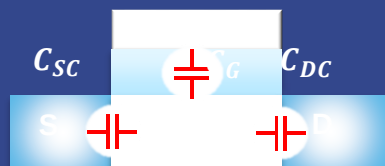
Top-4 Experimental TFETs	Channel Material	Structure (Channel Dimension)	$ V_{DS} $ (V)	SS_{min} (mV/dec)	SS_{avg} over 3 decades (mV/dec)	SS_{avg} over 4 decades (mV/dec)	I_{on} ($\mu A/\mu m$)	I_{on}/I_{off} Ratio
Tomioka et. al. (Hokkaido Univ./JST) Nano Letters 2013 Symp. on VLSI Technology 2012	Si/III-V Hetero-NW	NW (30 nm)	1	12	21	21	1	2×10^6
			0.1	N/A	21	>60	0.001	1×10^6
Gandhi et. al. (NUS/IME/UCSB) IEEE Elect. Dev. Lett. 2011 IEEE Elect. Dev. Lett. 2011	Si-NW	NW (30-40 nm)	0.1	30	50	>60	0.003	1×10^4
		NW (18 nm)	0.1	30	50	>60	0.44	1.6×10^5
Jeon et. al. Symp. on VLSI Technology 2010 (SEMATECH/Berkeley/Texas State Univ.)	Si	SOI (40 nm)	1	32	~ 55	>60	1.2	6×10^6
Kim et. al. (Berkeley) Symp. on VLSI Technology 2009	Si	SOI (70 nm)	0.5	38	~ 50	>60	0.42	3.5×10^6

Advantages of 2D Materials for TFETs

W. Cao, D. Sarkar, Y. Khatami, J. Kang and K. Banerjee, AIP Advances, 4, 067141, 2014.

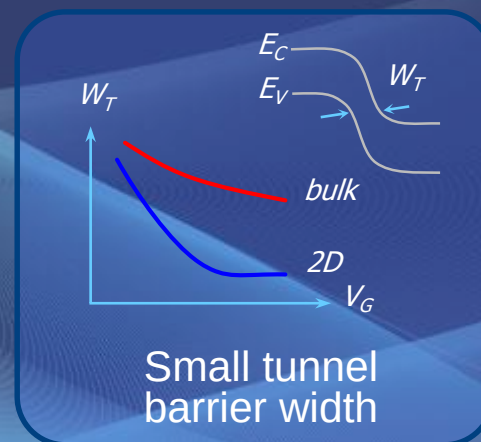
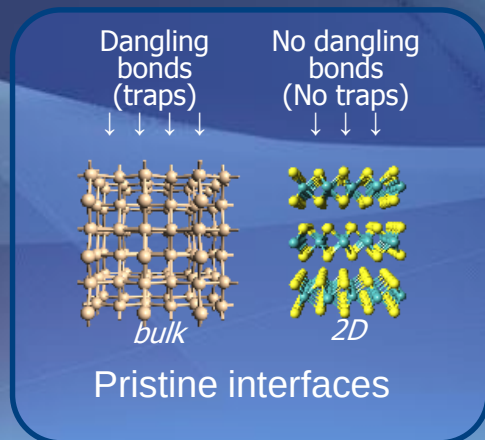
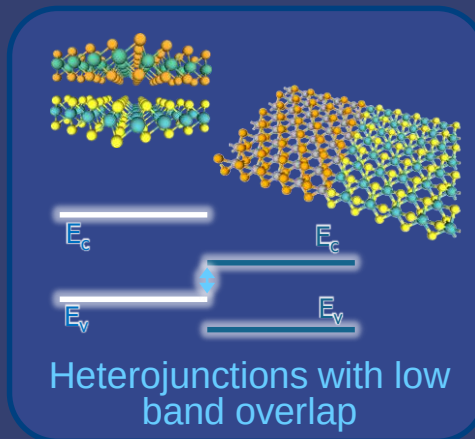
$$SS = \frac{\partial V_{GS}}{\partial \psi} \frac{\partial \psi}{\partial \log(I_D)}$$

electrostatics current modulation efficiency



$$V_{ch} = \frac{C_G}{C_G + C_{SC} + C_{DC}} V_G$$

Better electrostatics

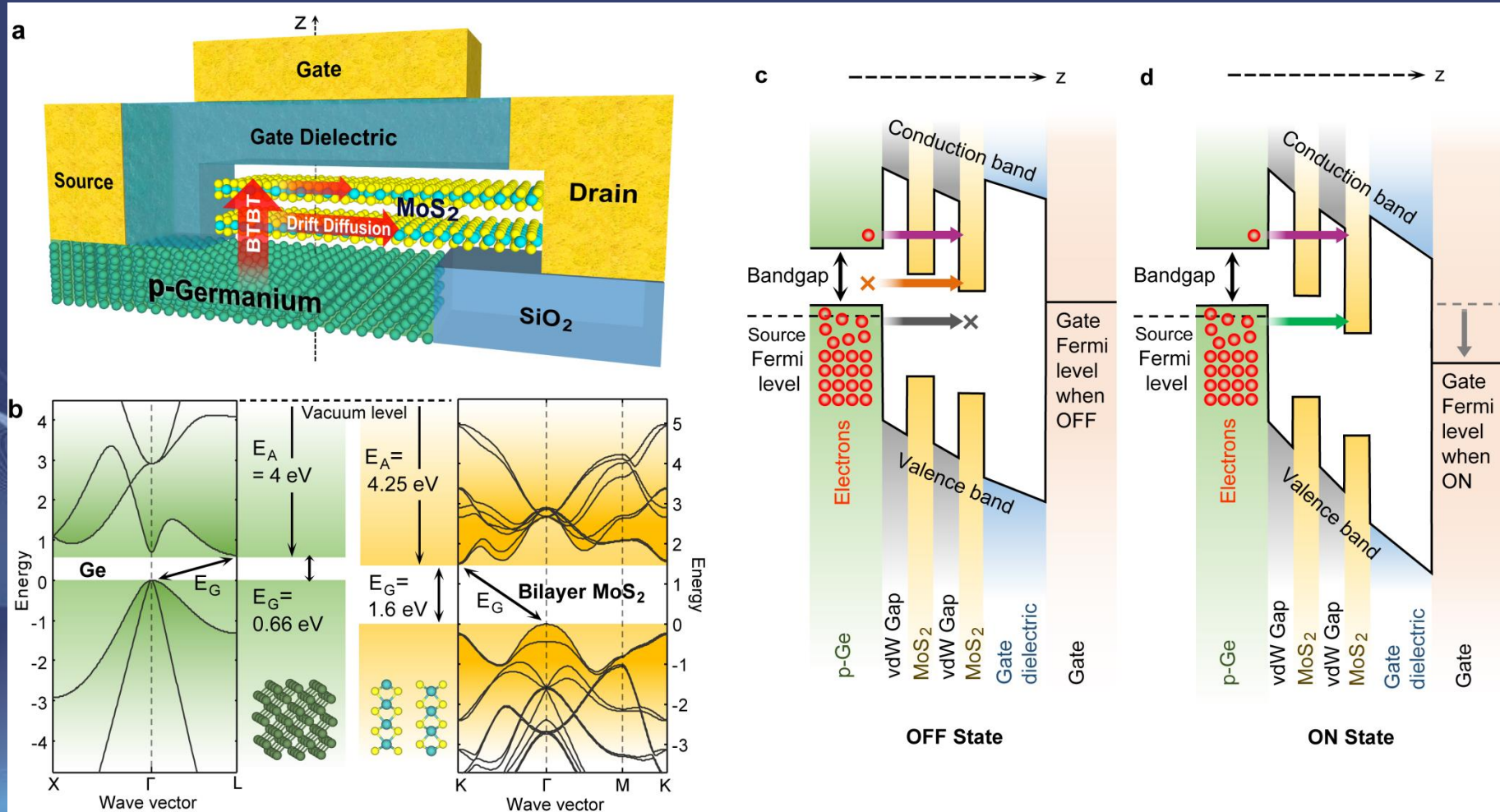


Higher Tunneling Current

Planar Platform: easy to process

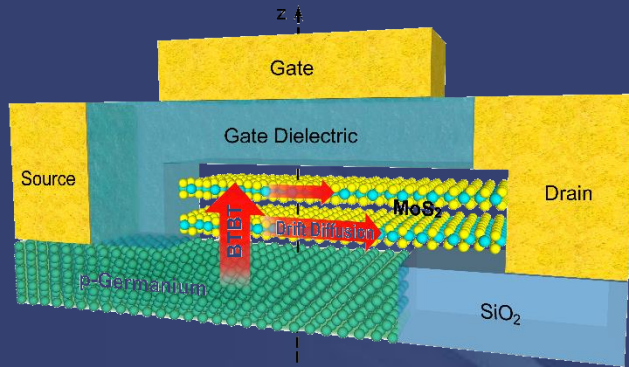
ATLAS-TFET: First 2D-Channel Tunnel FET

Nature, 526, 91-95, Oct 1, 2015.

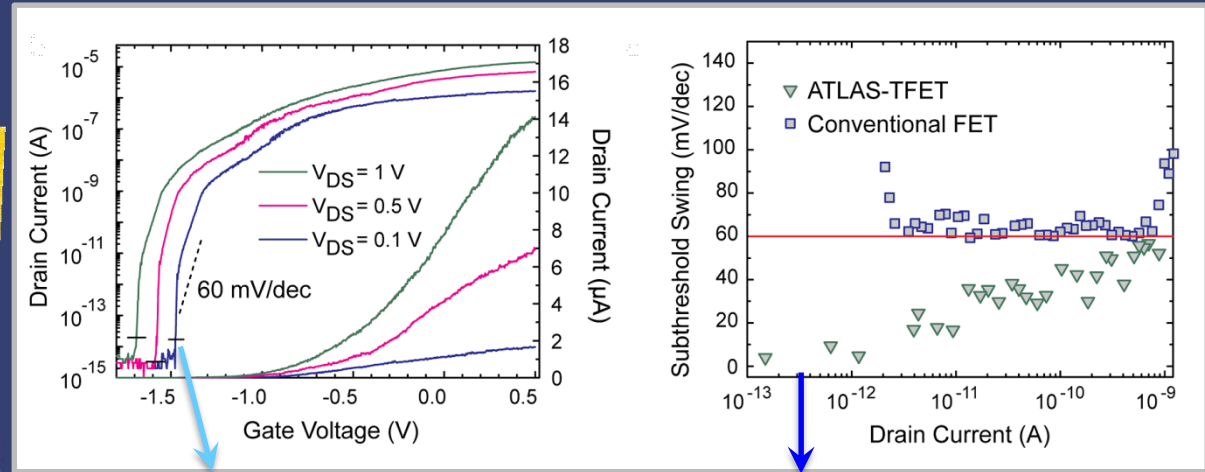


ATLAS-TFET: Thinnest & Greenest Transistor

Nature, 526, 91-95, Oct 1, 2015.



**World's Thinnest
Channel Transistor
with Subthermionic
SS!!**



**Minimum SS of 3.9
mV/dec**

**Average SS of 31.1
mV/dec for 4 decades**

- Uniquely combines the advantages of 3D (high doping) and 2D (ultra-thin & pristine)
- Ge-MoS₂ provides a staggered band alignment— reduced tunnel barrier height
- Bilayer MoS₂— ultra-thin tunnel barrier width, reduced scattering, higher DOS
- Vertical van der Waals heterostructure— large tunneling area, negligible diffusion of dopants (vdW gap) leading to high electric field across source-channel junction

ONLY TFET to achieve *subthermionic* SS over four decades of drain current, at V_{DD} of 0.1 volts, with over 2X improvement in ON current!!!!