# Sub-50 nm P-Channel FinFET

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***Abstract*—High-performance PMOSFETs with sub-50–nm gate-length are reported. A self-aligned double-gate MOSFET structure (FinFET) is used to suppress the short-channel effects. This vertical double-gate SOI MOSFET features: 1) a transistor channel which is formed on the vertical surfaces of an ultrathin Si fin and controlled by gate electrodes formed on both sides of the fin; 2) two gates which are self-aligned to each other and to the source/drain (S/D) regions; 3) raised S/D regions; and 4) a short (50 nm) Si fin to maintain quasi-planar topology for ease of fabrication. The 45-nm gate-length p-channel FinFET showed an $I_{\rm dsat}$ of 820 $\mu$A/$\mu$m at $V_{\rm ds} = V_{\rm gs} = 1.2$ V and $T_{\rm ox} = 2.5$ nm. Devices showed good performance down to a gate-length of 18 nm. Excellent short-channel behavior was observed. The fin thickness (corresponding to twice the body thickness) is found to be critical for suppressing the short-channel effects. Simulations indicate that the FinFET structure can work down to 10 nm gate length. Thus, the FinFET is a very promising structure for scaling CMOS beyond 50 nm.**

***Index Terms*—Double-gate MOSFETs, fully depleted, MOS devices, scaled CMOS, short-channel effect, silicon-germanium (SiGe), SOI MOSFETs.**

## I. Introduction

SCALING of device dimensions has been the primary factor driving improvements in integrated circuit performance and cost, which have led to the rapid growth of the semiconductor industry. Due to limitations in gate-oxide thickness and source/drain(S/D) junction depth, scaling of conventional bulk MOSFET devices well beyond the 0.1-$\mu$m process generation will be difficult if not impossible [1]. New device structures and new materials will be needed to overcome the technological challenges.

The double-gate MOSFET is considered the most attractive device to succeed the planar MOSFET [2]. With two gates controlling the channel, short-channel effects can be greatly suppressed. The FinFET, a recently reported novel double-gate structure, consists of a channel formed in a vertical Si fin controlled by a self-aligned double-gate [3]–[5]. The fin is made thin enough when viewed from above such that the two gates control the entire fully-depleted channel film. Self-alignment is necessary for reducing parasitic gate capacitances, series resistance and for control of the channel length. Fig. 1 shows the FinFET structure in this process, which features 1) a channel which is formed on the vertical surfaces of an ultrathin Si fin and controlled by gate electrodes formed on both sides of the fin; 2) two gates which are self-aligned to each other and to the S/D regions; 3) raised S/D for reduced parasitic resistance; and 4) a short (50 nm) Si fin to maintain quasi-planar topography for ease of fabrication. The following describes some critical dimensions of the FinFET structure in this process:

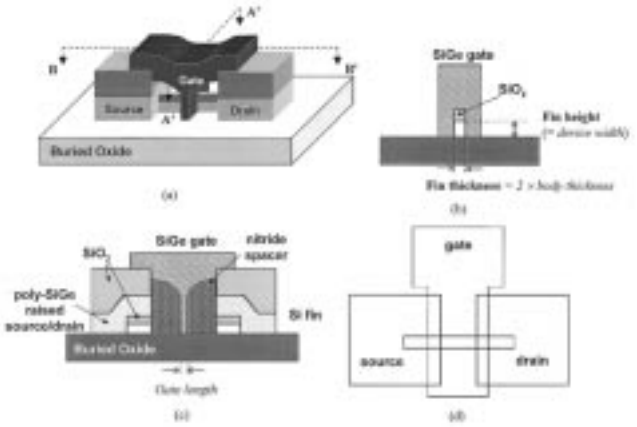


Fig. 1. FinFET structure. (a) Three-dimensional schematic spacers between source and drain are not shown in order to reveal the fin structure. (b) Cross-sectional view along A-A′. (c) Exploded view along B-B′. (d) Layout.

**Gate Length**: In this process, the physical gate length of the FinFET is defined by the spacer gap [Fig. 1(c)].

**Device Width**: Because the current flows along the vertical surfaces of the fin, the width of the FinFET equals the fin height [Fig. 1(b)]. (The top surface of the fin is covered by a thick oxide hard-mask and is not part of the channel.) This width definition only counts one side of the channel, which is the typical definition for double-gate devices [6], [7].

**Body Thickness**: Because there are two gates controlling both sides of the fin, the fin thickness for FinFET devices equals twice the body thickness [Fig. 1(b)].

Although it is a double-gate structure, the FinFET is similar to the conventional planar MOSFET in layout [Fig. 1(d)] and fab-

Manuscript received January 20, 2000; revised October 4, 2000. This work made use of the National Nanofabrication Users Network Facilities funded by the National Science Foundation under Award ECS-9731294. This work was supported by the DARPA AME Program under Contract N66001-97-1-8910. The review of this paper was arranged by Editor K. Shenai.

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Publisher Item Identifier S 0018-9383(01)02358-9.

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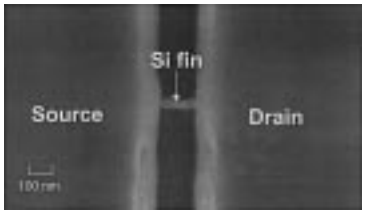


Fig. 2. SEM top view after S/D etch. A thin fin is visible in the gap between source and drain and will be further thinned by sacrificial oxidation.

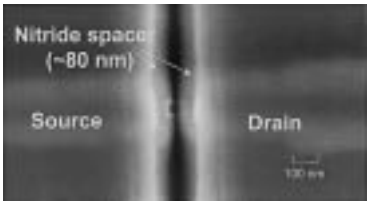


Fig. 3. SEM top view after nitride spacer etch. Si fin is at the center of the photo. The gap between spacers at the sides of the fin is less than 20 nm. This gap defines the gate length.

rication. It provides a range of channel lengths, CMOS compatibility and large packing density compared to other double-gate structures [6], [7].

N-channel FinFETs have been reported to show good short-channel performance down to a gate-length of 17 nm [4]. We have recently reported high-performance sub-50 nm p-channel FinFETs [5]. These results indicate that the FinFET is a promising device structure for future CMOS technology.

In this paper, the fabrication and performance of p-channel FinFETs are presented. Device simulations show good agreement with measured data, and predict good performance down to 10 nm gate length.

## II. Device Fabrication

The FinFET fabrication process used in this work is very similar to the process reported in [3]. The major differences are summarized in the second to last paragraph of this section. The first fabrication step is Si fin formation. A 100-nm SOI film was thinned to 50 nm by thermal oxidation. The measured standard deviation of the silicon film thickness was around 2 nm. Ion implantation established a body doping concentration of $10^{16}$ cm$^{-3}$. Then LTO was deposited over the Si film as a hard mask for etching. It also protected the Si fin through subsequent process steps. Using 100 keV e-beam lithography and resist ashing in $O_2$ plasma, narrow Si fins were patterned. The fin height is equal to the thickness of the SOI film—50 nm. As explained in the previous section, the FinFET channel width is equal to the fin height, so that a single-fin device has a width of 50 nm. The resulting fin thickness ranged from 30 nm to 150 nm. The final Si fin thickness ($<$ 10 nm–120 nm) was smaller because of thinning during subsequent dry-etching and oxidation processes.

The second step is S/D formation. A 100-nm *in-situ* boron-doped $Si_{0.85}Ge_{0.15}$ and a 300-nm LTO hard mask were deposited over the fin. SiGe was used for the raised S/D because it has lower resistivity and is a good dopant diffusion source [8], [9]. The $Si_{0.85}Ge_{0.15}$ provides good electrical contact along the side surfaces of the Si fin. The LTO and SiGe films were etched to delineate and separate the raised source and drain regions. By sufficient overetching, the poly-$Si_{0.85}Ge_{0.15}$ stringers beside the Si fin were completely removed, with the Si fin protected by the oxide hard mask. Fig. 2 shows the top-view SEM picture of the S/D with a gap in-between and a visible Si fin covered by the hard mask.

The third step is nitride spacer formation. 100 nm LPCVD nitride was deposited and etched to form spacers on the sidewalls of the S/D. By sufficient overetching, nitride was removed from the sidewalls of the fin. Fig. 3 shows a gap less than 20 nm between the S/D spacers. (The fin is difficult to see at the center.) The width of this spacer gap at the sides of the fin (not the top of the fin/hardmask) determines the gate length.

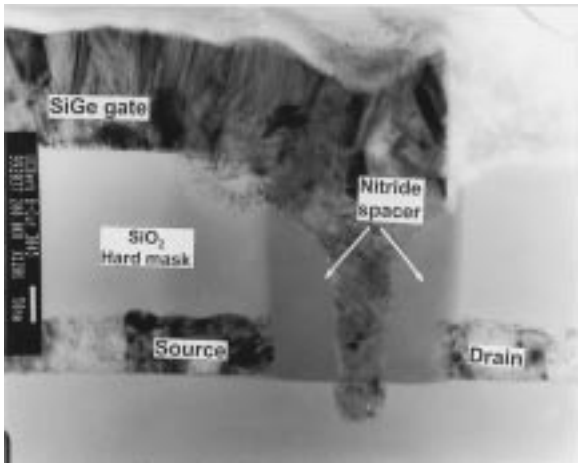


Fig. 4. Cross-sectional TEM picture: gate is defined by the gap between nitride spacers. Excellent vertical gate and spacer profiles are shown.

The fourth step is gate-oxide formation. 15 nm of sacrificial oxide was grown and wet etched to remove the damage created by the dry-etching processes on the side surfaces of the fin. This step further reduces the fin thickness. The final thickness of the fins ranged from less than 10 nm to 120 nm. 2.5 nm gate oxide was grown on the side surfaces of the fin at 750 °C. This "high-temperature" step, combined with an additional annealing step, drove boron from the SiGe raised S/D regions into the fin underneath the nitride spacers to form $P^+$ S/D extensions.

To adjust the threshold voltage of ultrathin body SOI MOSFETs, gate work-function tailoring is essential. This is because light body doping is used so that the depletion charge in the channel contributes negligibly to the threshold voltage. The threshold voltage is therefore insensitive to dopant fluctuations in the channel. The fully depleted body design suppresses the floating body effect, and mobility is improved as well. $P^+$ $Si_{0.4}Ge_{0.6}$ with a work function of 4.75 eV [10] was used in the devices fabricated in this work. 200 nm of *in-situ* doped $Si_{0.4}Ge_{0.6}$ was deposited by LPCVD and patterned to form the gate electrode. The cross-sectional TEM picture in Fig. 4 shows excellent vertical gate and spacer profiles. The gate length of the TEM test structure, which is approximately 50 nm, as seen in Fig. 4, is drawn longer than that of the actual devices.

The $Si_{0.4}Ge_{0.6}$ gate straddles the fin and the conducting channels are formed on the sides of the fin. Because the S/D and

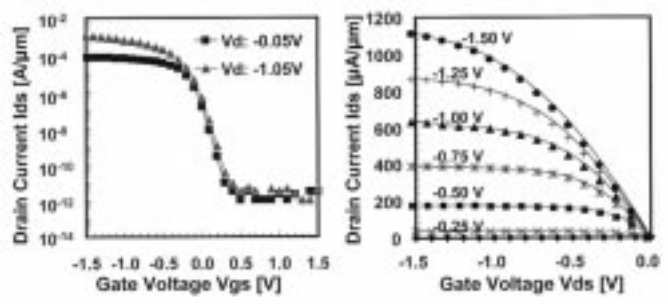


Fig. 5. $I$–$V$ characteristics for p-channel FinFET with 45- nm gate length and 30 nm Si body. $I_{\rm dsat}$ is or 820 $\mu$A/$\mu$m at $V_{\rm ds} = V_{\rm gs} = 1.2$ V.

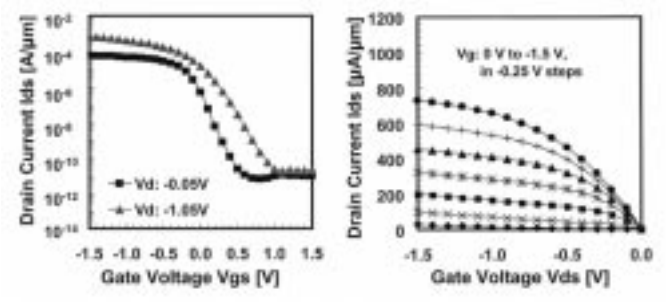


Fig. 6. $I$–$V$ characteristics for PMOS FinFET with 18 nm gate length and 20 nm Si body. $I_{\rm dsat}$ is 576 $\mu$A/$\mu$m at $V_{\rm ds} = V_{\rm gs} = 1.2$ V.

gate are much thicker (taller) than the fin, the device structure is quasi-planar.

The last step is S/D contact etching. Windows were etched through the oxide hardmask to allow for direct probing of the poly-SiGe source and drain pads. Finally, a forming-gas anneal at 400 °C was performed. No metallization was used in this experiment to allow for the option of further thermal annealing.

The major process modifications from [3] include: 1) addition of the sacrificial oxidation step before growing gate oxide to improve the interface quality; 2) use of nitride as the spacer material instead of oxide to increase the etch process window; and 3) use of SiGe for the elevated S/D instead of Si for lower sheet resistance and as a better diffusion source. As a result, much better device performance (reported in Section III) is achieved in this work as compared to [3].

The process described here is for p-channel FinFET fabrication. To adapt this process to CMOS technology, masked ion implantation steps would be required to dope the S/D regions, and different gate materials may be needed for the n-channel and p-channel devices in order to achieve the desired threshold voltages.

## III. Device Performance and Discussion

Fig. 5 shows the $I$–$V$ characteristics of a 45-nm physical gate length device with a 30-nm thick Si fin. $I_{\rm dsat}$ is 820 $\mu$A/$\mu$m at $V_{\rm ds} = V_{\rm gs} = 1.2$ V. A low subthreshold swing of 69 mV/dec was achieved, indicating that short-channel characteristics are well controlled by the use of a thin fin. Fig. 6 shows the $I$–$V$ characteristics of an 18 nm gate-length device with a 20 nm thick Si fin. $I_{\rm dsat}$ is 576 $\mu$A/$\mu$m at $V_{\rm ds} = V_{\rm gs} = 1.2$ V. $I_{\rm dsat}$ for this device is smaller than for the 45 nm device due

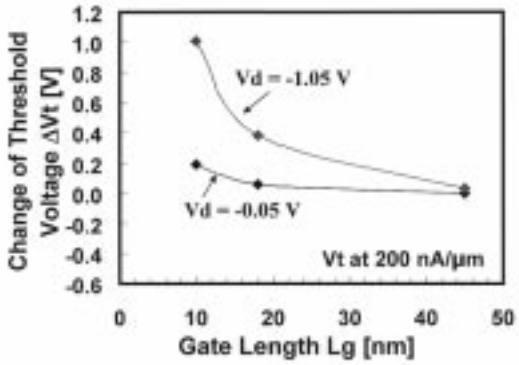


Fig. 7. $Vt$ roll-off characteristics for both linear ($V_{\rm ds} = -0.05$ V) and saturation regions ($V_{\rm ds} = -1.05$ V). Good short-channel behavior is shown down to a gate length of 18 nm.

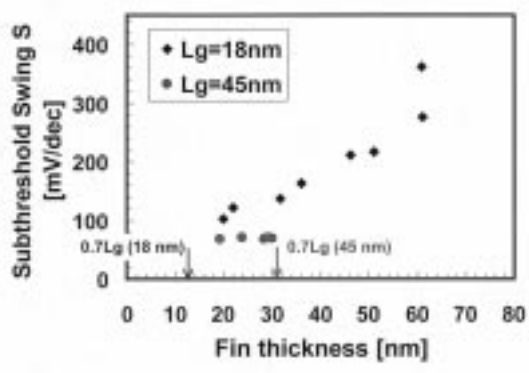


Fig. 8. Subthreshold swing versus fin thickness. Small fin thickness (thin body) is critical for suppressing short-channel effects.

to its thinner fin, which yields larger series resistance. The subthreshold swing and DIBL can be expected to improve with the use of a thinner gate oxide (current gate oxide thickness is 2.5 nm for all devices). To our knowledge, this is the shortest gate length p-channel MOSFET demonstrated to date.

$Vt$ roll-off characteristics for both linear and saturation regions are shown in Fig. 7. $Vt$ is defined as the gate voltage when $I_{\rm ds} = 200$ nA/$\mu$m. Despite the relatively thick gate oxide (2.5 nm), the FinFET shows very high drive current and good short-channel behavior down to a gate length of 18 nm. This is because the FinFET structure, with its double gate and thin body, effectively suppresses DIBL and thus relaxes the gate-oxide scaling requirement. This is a great advantage because oxide scaling has become one of the limiting factors in conventional MOSFET scaling, due to gate leakage current.

Fig. 8 shows the subthreshold swing dependence on the Si-fin thickness. For FinFET devices with gate-length of 18 nm, the subthreshold swing worsens with increasing fin thickness, which corresponds to twice the body thickness. For a gate-length of 45 nm, FinFET devices show small subthreshold swing even with a 30 nm thick fin. From these results, it appears that a fin thickness as large as 70% of the gate length is effective for suppressing short-channel effects, for the light body doping and S/D design used in this study.

Fig. 9 shows the temperature dependence of the drive current. It is observed that the drive current is reduced as the temperature goes down. This is opposite to the usual MOSFET behavior. It

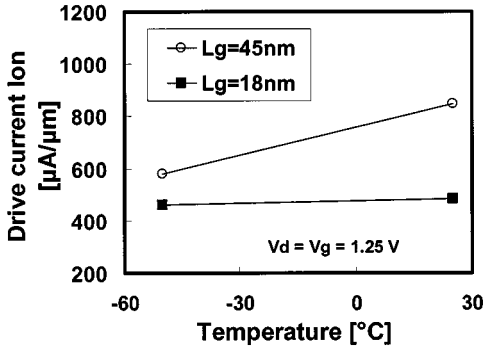


Fig. 9. Temperature dependence of drive current.

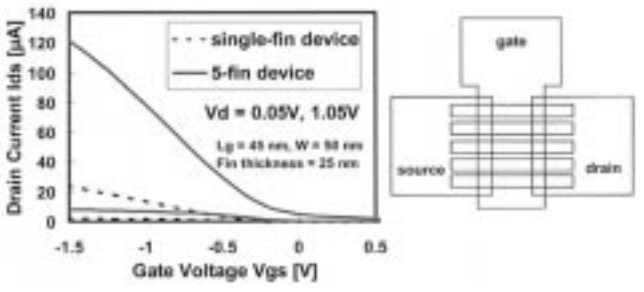


Fig. 10. FinFET width can be adjusted quasi-continuously by the increment of a single fin. The 5-fin device conducts five times the current of the single-fin device. Measurement results and the layout for a 5-fin device are shown.

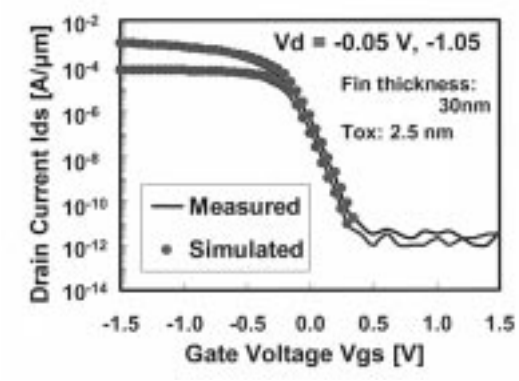


Fig. 11. Comparison between simulation data and experimental data.

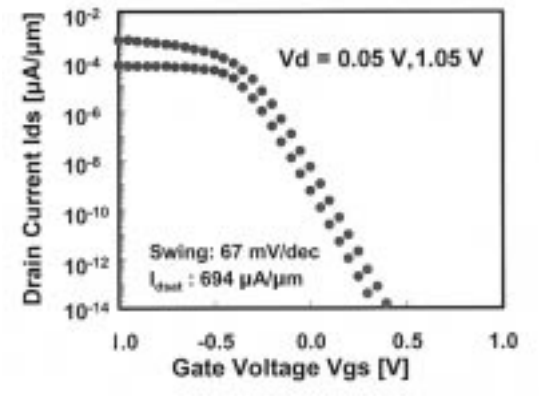


Fig. 12. Simulation data for FinFET with 10-nm gate-length. $I_{\rm dsat} = 694\ \mu$A/$\mu$m for $V_{\rm gs} = V_{\rm ds} = 1.2$ V, and $I_{\rm off} = 4.6$ nA/$\mu$m.

is tempting to take this as an indication of ballistic transport. However the gate-length dependence does not support this interpretation. Because ballistic transport will be more significant for shorter-channel devices, we would expect to see more current reduction for the $Lg = 18$ nm device as the temperature is decreased. However, the experimental results show just the opposite, with more current reduction in the longer channel device ($Lg = 45$ nm) and only marginal reduction in the shorter channel device ($Lg = 18$ nm). Further study is needed to elucidate this temperature effect.

The self-aligned process and the quasi-planar structure of the FinFET make it amenable to achieving larger effective channel width by increasing the number of Si fins. The S/D pads straightforwardly connect the fins in parallel. Multi-fin devices were fabricated and results are presented in Fig. 10. The 5-fin device conducts five times the current of the single-fin device. Although the channel width can be varied only in increments of twice the fin height, this is not a serious design constraint because the increment is small (0.1 $\mu$m) in the current process. If closely-spaced Si fins can be fabricated with an advanced lithography tool, the FinFET structure can be used to attain ultrahigh-density integrated circuits.

The data obtained in this experiment closely matches two-dimensional device simulations which assume simple Gaussian S/D doping profiles and a uniformly doped channel region. The drift-diffusion model underestimates the current by 15% for the 45 nm device. The energy balance model was found to give excellent agreement with experimental data. Fig. 11 shows the comparison between experimental and simulation data for both the on-state and off-state currents. It was found that quantum models are not needed in order to obtain good agreement between experimental and simulation results. Therefore quantum mechanical effects do not seem to be significant at this dimension.

Employing the same simulation model and S/D dopant profiles which match experimental results of the 45 nm and 18 nm devices, the performance of a 10 nm FinFET was simulated (Fig. 12). By aggressively scaling the gate-oxide thickness (1.2 nm) and the silicon fin thickness (7 nm), a drive current of 694 $\mu$A/$\mu$m can be achieved at $V_{\rm ds} = V_{\rm gs} = 1$ V, while still maintaining low leakage (4.6 nA/$\mu$m) and minimal short channel effects. This is due to the excellent short-channel behavior of the FinFET structure. There are two effects not considered in the simulation which might be of importance at this small dimension: quantum effects and ballistic transport. In principle, quantum effects may decrease the mobility by $\sim$10% [11]. On the other hand, ballistic transport may increase the current by $\sim$20%.

## IV. Conclusions

Sub-50 nm p-channel FinFETs, in which the channels are formed in vertical ultrathin Si fins and controlled by self-aligned double-gates, were successfully fabricated. These devices exhibited high drive currents (820 $\mu$A/$\mu$m) at $V_{\rm ds} = V_{\rm gs} = 1.2$ V for $Lg = 45$ nm and good performance down to $Lg = 18$ nm. Simulation results indicate that this structure should be scalable

down to 10 nm. The formation of an ultrathin fin ($<0.7\ Lg$, for a lightly doped body) is critical for suppressing short-channel effects. This structure was fabricated by forming the S/D before the gate, a technique that may be needed for future high-K-dielectric and metal-gate technologies that cannot tolerate the high temperatures required for S/D formation. Further performance improvement is possible by using a thinner gate dielectric and thinner spacers. Despite its double-gate structure, the FinFET is similar to the conventional MOSFET with regard to layout and fabrication. It is an attractive successor to the single-gate MOSFET.

## ACKNOWLEDGMENT

The authors would like to thank the UC Berkeley Microfabrication Laboratory staff for their support in device fabrication.

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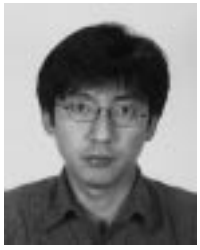

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