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CMOS Design Challenges to Power Wall

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Introduction

CMOS power dissipation has been increasing due to the increase in power density as shown in Fig. 1. The power dissipation increased fourfold every three years until the early 1990's, due to a constant voltage scaling. Recently, a constant field scaling has been applied to reduce power dissipation, where the power density is increased proportional to the 0.7th power of scaling factor, resulting in power increase by twice every 6.5 years. It is considered that the power dissipation of CMOS chips will steadily be increased as a natural result of device scaling.

Technology scaling will become difficult due to the power wall. On the other hand, future computer and communications technology will require further reduction in power dissipation. Since no new energy efficient device technology is on the horizon, low power CMOS design should be challenged. This paper discusses what and how much designers can do for CMOS power reduction [1].

Low Power Design Techniques

A. Lowering Supply Voltage

In order to maintain chip performance at low supply voltages (V_{DD}'s), there are three approaches: (a) utilize parallel and/or pipeline architectures to compensate for the degraded circuit speed, (b) lower threshold voltage (V_{TH}) to recover the circuit speed, and (c) lower V_{DD} only for non-critical circuits. In the second approach V_{DD} and V_{TH} should be optimized according to speed requirement from time to time (hence, variable), while in the third approach they should be optimized spatially from circuits to circuits (hence, multiple).

A Variable Threshold-voltage CMOS technology (VTCMOS) [2] is developed to control V_{TH}, and a Variable Supply-voltage (VS) scheme [3] is investigated to control V_{DD}. These two research achievements give IC designers freedom of controlling V_{DD} and V_{TH} for better trade-offs between power and speed, while they were given as boundary conditions and unchangeable parameters in conventional design. A RISC core with the VS scheme in VTCMOS is designed. Measured performance in MIPS/W is improved by a factor of more than 2 compared with that of a conventional design, as depicted in Fig. 2. Chip leakage current is controlled for active and standby modes independent of processed V_{TH}.

Two MPEG-4 vide codec chips are developed [4][5]. Measured power dissipation is depicted in Fig. 3. By optimizing V_{DD} and V_{TH}, V_{DD} can be lowered to 2.5V from 3.3V so that power dissipation is reduced by 43%. By employing one more V_{DD}, 1.75V, for non-critical circuits, power dissipation is further reduced by 25%, in total by 55% compared to a conventional design at 3.3V.

Design knowledge on multiple V_{DD}'s and V_{TH}'s are reported in [6]. Power reduction by multiple V_{DD}'s is about 50%. The more V_{DD}'s, the less power dissipation, but the effect will be saturated very soon. Leakage reduction by multiple V_{TH}'s is about one or two orders of magnitude. The leakage reduction effect will also be saturated as the number of V_{TH} increases.

B. Lowering Capacitance

External memory access consumes considerable power dissipation due to large parasitic capacitance along external signal lines. An MPEG-4 videophone LSI with 16Mbit embedded DRAM is fabricated in a 0.18μm embedded DRAM process [7]. Power dissipation is reduces to one third of the total power dissipation of a two-chip solution, as depicted in Fig. 4.

C. Lowering Switching Activity

Flip-flops, key circuits to synchronous design, consume large and increasing amount of total chip power dissipation. In a conventional flip-flop, half of the total transistors are subject to consume ac power, even when input data is unchanged. A conditional flip-flop circuit is developed where internal clock is activated only when a new input data arrives [8]. A discrete cosine transform (DCT) block for the MPEG-4 video codec is designed and fabricated with this conditional flip-flop. The chip consumes 24%-51% less power without speed degradation compared to a conventional design, as depicted in Fig. 5.

D. Impact to CMOS life span

CMOS power dissipation can be reduced to x0.8-x0.5 by lowering supply voltage, x0.8-x0.3 by lowering capacitance, and x0.8-x0.5 by lowering switching activity. In total, power reduction to x0.5-x0.1 can be achieved by design efforts. Suppose the natural power increase due to device scaling by twice every 6.5 years, this power reduction corresponds to expansion of CMOS life span by about 6-20 years.

System Perspective

It is expected that paradigm shifts by downsizing will continue to be experienced in the computer industry. $200 portable computers, $20 wearable computers, and even $2 implantable computers for personal applications in many spheres of life are in prospect.

As computers are downsized, communications technology for connecting them to network becomes more essential. LAN will invade from office into home. Personal Area Network (PAN) will then evolve.

Ubiquitous computing in Fig. 6 is a next genet information technology where computers and communications will be scaled further, merged together, and materialized in consumer applications. Computers will be invisible behind broadband networks as servers, while terminals will come closer to people as wearable/implantable devices, more friendly devices with sophisticated human-computer-interactions. IC chips will be implanted everywhere so that things can think and talk for distributed information processing. Key technologies here are low power, low cost, and good interface especially for wireless data communications.

Conclusion

Power wall is a clear and present roadblock in the semiconductor industry. Even though design challenges should further be taken, a new set of technology is strongly required for mass production in the 2010's as a long-term solution to the power problems. It is hoped that innovations will occur as they did before. To this end, it is important to know the impact of the evolution of integrated circuits to our society, and to promote research efforts of the world.

Acknowledgement

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References

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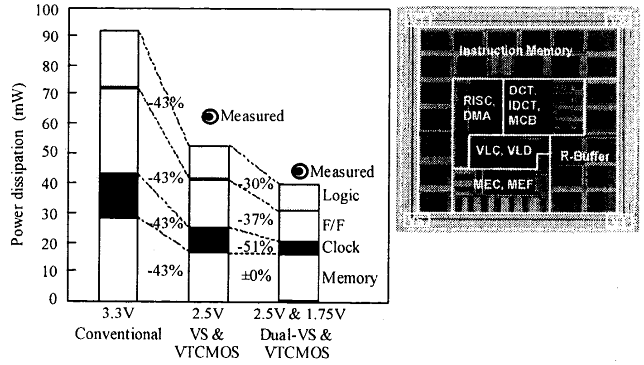


Fig. 3 Power reduction in dual-V_{DD} and VTCMOS technology.

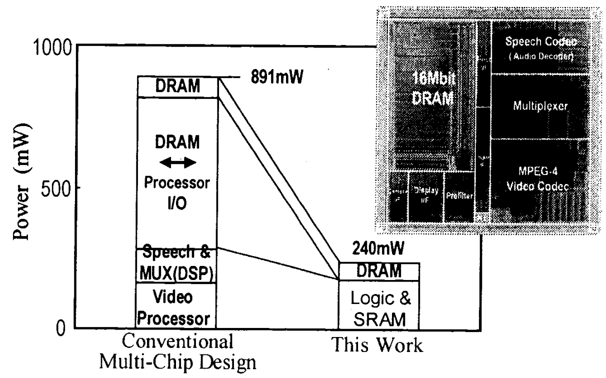
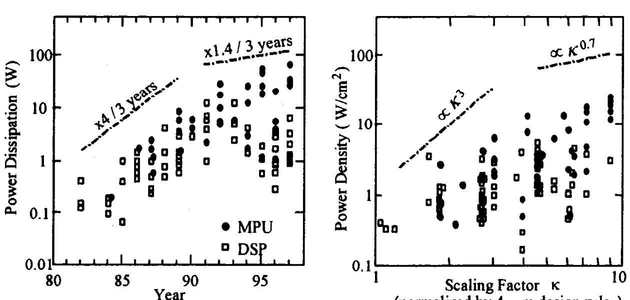
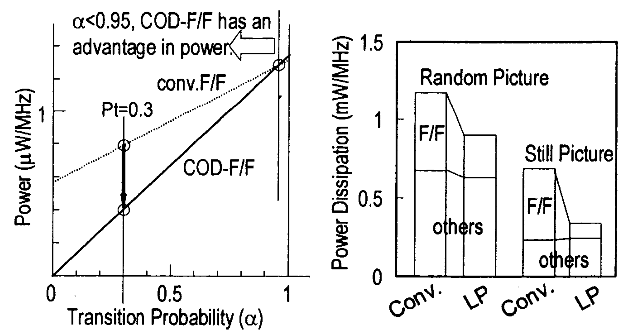


Fig. 4 Embedded DRAM for capacitance reduction.



(a) Power dissipation vs. year. (b) Power density vs. scaling factor.

Fig. 1 Power increase due to device scaling.



(a) Power dissipation vs. transition probability. (b) Power reduction in MPEG-4 chip.

Fig. 5 Conditional Flip-Flop for lowering switching activity.

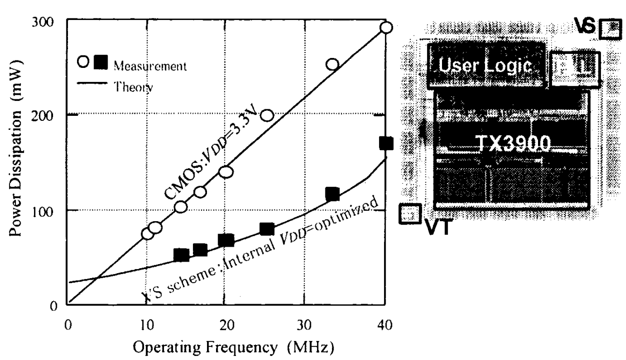


Fig. 2 Power reduction using variable-V_{DD}, V_{TH} technology.

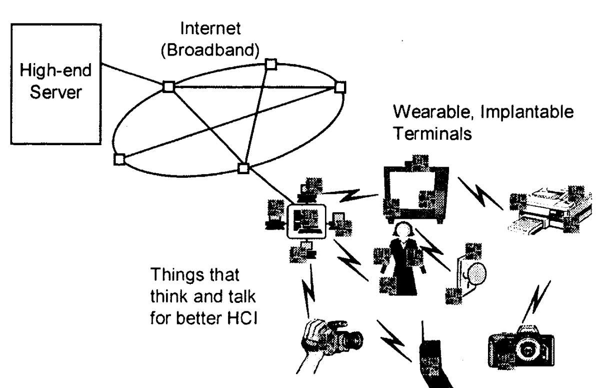


Fig. 6 Ubiquitous computing.