Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing ($\leq$ 50 mV/decade) at Room Temperature

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***Abstract*—This letter presents a Si nanowire based tunneling field-effect transistor (TFET) using a CMOS-compatible vertical gate-all-around structure. By minimizing the thermal budget with low-temperature dopant-segregated silicidation for the source-side dopant activation, excellent TFET characteristics were obtained. We have demonstrated for the first time the lowest ever reported subthreshold swing (SS) of 30 mV/decade at room temperature. In addition, we reported a very convincing SS of 50 mV/decade for close to three decades of drain current. Moreover, our TFET device exhibits excellent characteristics without ambipolar behavior and with high $I_{\text{on}}/I_{\text{off}}$ ratio ($\sim 10^5$), as well as low Drain-Induced Barrier Lowering of $\sim$70 mV/V.**

***Index Terms*—CMOS technology, gate-all-around (GAA), subthreshold swing (SS), top–down, tunneling field-effect transistor (TFET), vertical silicon nanowire (NW) (SiNW).**

I. Introduction

THE PERFORMANCE of metal–oxide–semiconductor field-effect transistors (MOSFETs) has degraded over the years due to their aggressive scaling. One of their important figures of merit is the subthreshold swing (SS), which is defined as the change in gate voltage required for a change of an order of magnitude of current from OFF to ON state. The SS of a MOSFET is governed by thermionic emission-carrier diffusion over a thermal barrier and limited to 60 mV/decade at room temperature. Thus, further scaling down of MOSFET supply voltage is very difficult without significantly increasing the OFF-state current. For future generations of integrated circuits, there is a need for ultra low-power and energy-efficient transistors with SS below 60 mV/decade. Recently, tremendous efforts have been made to create new devices for ultra low-power applications. Of the different devices being considered, tunneling field-effect transistor (TFET) is a promising candidate for such applications, as it can provide low OFF-state leakage, as well as SS below the 60 mV/decade limit of conventional MOSFETs [1]–[10]. In TFETs, the carrier transport is dictated by tunneling through a barrier instead of diffusion over the barrier as in conventional MOSFETs. In addition, for future CMOS applications, vertical gate-all-around (GAA) nanowire (NW) transistors are considered as a promising candidate due to excellent gate-to-channel coupling, high integration for circuit functionality, and compatibility with the existing CMOS technology [11], [12]. In this letter, we present a vertical silicon-NW (SiNW) GAA TFET with a source-side dopant-segregated silicidation at low-temperature. The silicidation is performed to activate the source-side dopants and to achieve a steep dopant profile, which is important in achieving low SS. The resulting device has reduced ambipolar behavior, an SS of 50 mV/decade, a high $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^5$, and a low drain-induced barrier lowering (DIBL) of $\sim$70 mV/V. An SS of 30 mV/decade has also been obtained, although only for little more than one decade.

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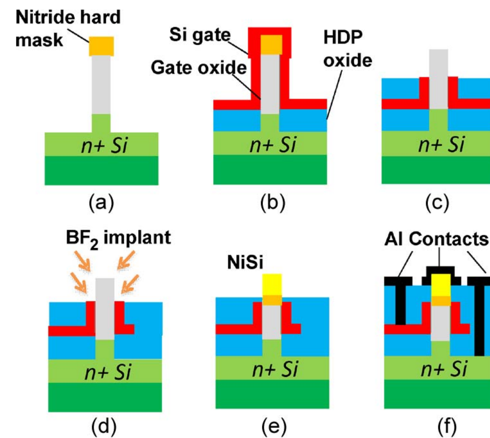

Fig. 1. Vertical silicon-NW TFET process flow schematic. (a) Vertical pillar etch and As implantation to form the drain region. (b) Isolation oxide deposition and gate stack formation. (c) Top amorphous Si etched to expose the source side of TFET. (d) Source implanted with BF_2. (e) Dopant-segregated Ni silicidation. (f) Contact opening and Al metallization.

II. Device Fabrication

N-Channel GAA silicon-NW-based TFETs were fabricated using a top–down CMOS-compatible process technology using the flow shown in Fig. 1. Silicon nitride (SiN) hard mask

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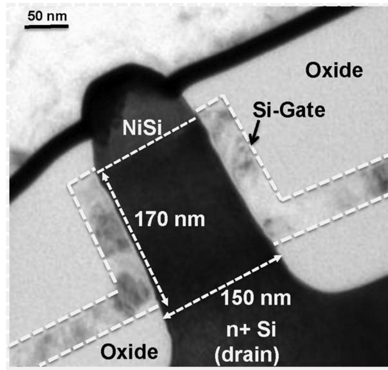

Fig. 2. Cross-sectional TEM image of a vertical SiNW TFET device with a diameter of ∼150 nm and a gate length of ∼170 nm.

was lithographically patterned on 8-in Si bulk p-type (boron $\sim 10^{15}$ cm^{-3}) wafers. Hard mask and 400-nm Si were anisotropically etched using deep RIE to form vertical Si NWs. Thermal oxidation at 1000 °C for 30 min, followed by the removal of grown oxide in diluted hydroflouric acid (DHF), was done to smoothen the NW surface and to reduce NW diameter. NWs with diameters ranging from 20 to 200 nm were obtained. After vertical NW formation, a vertical As implantation (10^{15} cm^{-2}/20 keV) was performed to define the drain region of the TFET [Fig. 1(a)]. The dopants were activated at 1000 °C for 10 s. Subsequently, 200 nm of high-density plasma (HDP) oxide was deposited and then followed by wet etch back using DHF. This resulted in ∼120 nm remaining HDP oxide to cover the footing of the vertical NW. Thereafter, a gate oxide of 4.5 nm was thermally grown on the exposed NW surface. Immediately after that, a 50-nm amorphous-Si gate material was deposited by LPCVD [Fig. 1(b)].

Gate was implanted vertically by using BF_2 (10^{15} cm^{-2}/10 keV) and activated at 1000 °C for 5 s. HDP oxide deposition and DHF etch back were performed, such that only the tip of the NW was exposed. The exposed top amorphous Si was then isotropically etched [Fig. 1(c)]. Gate pad serving as extension for gate contact was lithographically patterned and etched. BF_2 (10^{15} cm^{-2}/5 keV) was then implanted from four directions—90° apart at a tilt angle of 60° to form the p+ source region [Fig. 1(d)]. Isolation HDP oxide was again deposited and DHF etch back was once again used to create a spacer between gate edge and the source of NW.

Ni (15 nm) was deposited by sputtering and followed by a two-step rapid thermal annealing (RTA) at 220 °C/30 s and 440 °C/30 s in N_2 ambient. Unreacted Ni was selectively removed after the first RTA in $H_2SO_4 : H_2O_2 : H_2O$ solution, leaving NiSi around the source of NW [Fig. 1(e)]. Finally, contact holes were opened before Al metallization to form gate, source, and drain contacts [Fig. 1(f)]. Fig. 2 shows the cross-sectional TEM image of a fabricated TFET device with a diameter of 150 nm and a gate length of 170 nm. TEM was taken on larger diameter device for ease of sample preparation.

III. Results and Discussion

TFET is a gated p+-i-n+ diode operating under reverse bias. In the OFF state, the potential barrier between the source and the channel is large such that no tunneling occurs. On the other hand, in the ON state, the gate voltage pulls down the energy band of the channel region and reduces the width of the tunneling barrier. Because of this reduction in energy barrier, carriers can tunnel from the valence band of source to the conduction band of the channel region and thus constitute the tunneling current.

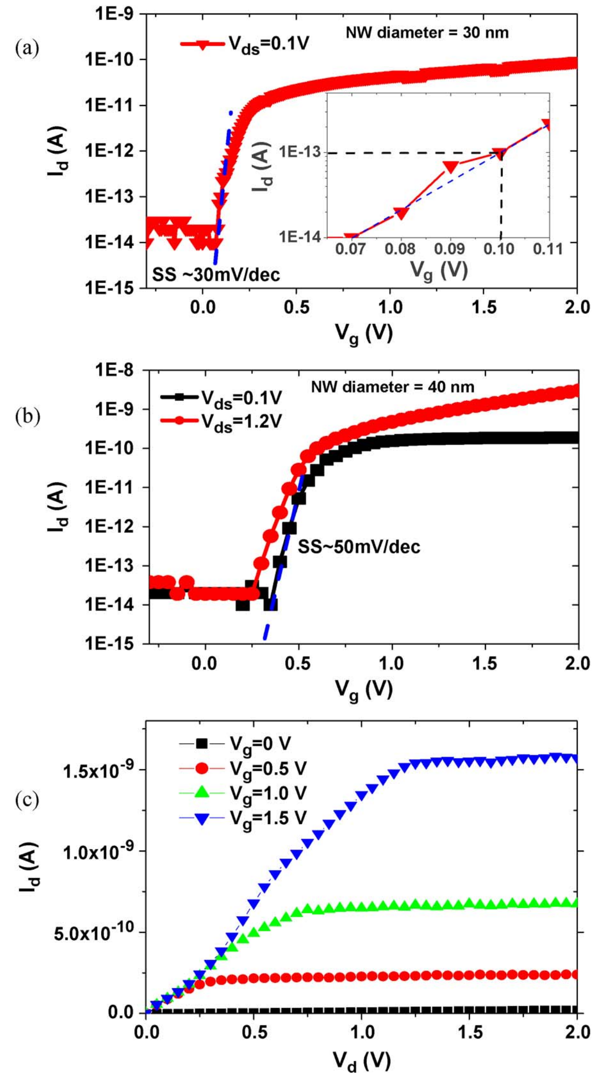

Fig. 3. (a) I_d–V_g characteristic of a vertical SiNW TFET with a low SS of 30 mV/decade. (b) I_d–V_g characteristic with an SS of 50 mV/decade over three decades of drain current. (c) Corresponding I_d–V_{ds} characteristics.

The TFETs in our experiment were characterized using the HP4156A parameter analyzer. Fig. 3(a) shows the input transfer characteristics of a SiNW TFET with a 30-nm diameter and a gate length of ∼170 nm. A low SS of 30 mV/decade is achieved for more than one decade of drain current. To the best of our knowledge, the SS of 30 mV/decade obtained in this letter is the lowest ever reported for any experimental TFET. The inset in Fig. 3(a) clearly shows the SS of 30 mV/decade for more than a decade of drain current. Another convincing result shown in Fig. 3(b) reveals that an SS of ∼50 mV/decade is achieved for close to three decades of drain current. There are not many experimental works on TFETs reporting an SS < 60 mV/decade for more than a decade of drain current. Excellent I_{on}/I_{off} ratio (10^5) is obtained, and also low DIBL

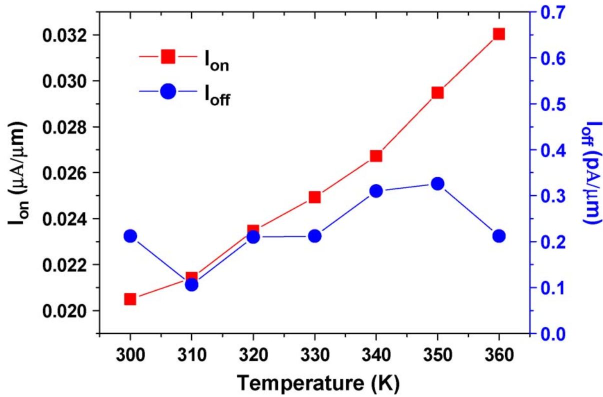

Fig. 4. I_{on} and I_{off} dependencies on temperature of SiNW TFET device with a diameter of ∼40 nm.

(∼70 mV/V) is achieved as a result of excellent gate control by GAA structure [4], [11], and [12]. The corresponding output characteristic is shown in Fig. 3(c). The TFET I_{on} is smaller compared to the conventional MOSFET I_{on} current. Large underlap on the drain side seems to be one of the reasons suppressing the ON current. Enhancement in the ON current is possible by using lower bandgap material at the tunneling interface [1], [5]–[9], as well as high-k gate insulator [8], [10].

It is worth mentioning here that the variation in SS behavior observed between the devices in Fig. 3(a) and (b) may be caused by process variations across the wafer. Edge silicide roughness, silicide encroachment, and variation in dopant density might cause the difference in SS. It should be noted that ambipolar conduction, which is an issue in TFET devices [3], [9], is not observed in our results. Unipolar NTFET characteristics are observed because of the asymmetric property of our TFET design. First, the source side has sharp doping profile as a result of dopant-segregated silicidation, which causes dopants to pile up at the silicide edge [13], [14]. The silicide interface in our TFET device is aligned with the gate, as shown in Fig. 2. Although the TEM image was taken on large wire diameter, for the smaller wire diameter, it is expected to have more NiSi encroachment into the narrower NW; therefore, silicide interface should have overlap or just be aligned with the gate. It should also be noted that, although a large difference in encroachment between wide and narrow pillars was found when doping is low, this difference was reduced when there was high doping in the pillars. The source side doping is enhanced by dopant segregation, thereby making the the doping gradient in the source-channel (p+-i) junction more abrupt. On the other hand, doping in the drain-channel (n+-i) junction at the bottom of NW is graded due to large thermal budget applied after vertical implant. This results in a much wider depletion region at the bottom tunneling junction and helps in reducing the ambipolar behavior.

Shown in Fig. 4 is the effect of temperature on TFET's I_{on} and I_{off} currents at $V_{\mathrm{ds}} = 1.2$ V. A small increase in I_{on} is observed as temperature increases. This can be explained by the increase in tunneling probability due to temperature-induced bandgap reduction [15], change in Fermi function, and phonon interactions. This is unlike a MOSFET in which I_{on} degrades with increasing temperature. Meanwhile, I_{off} exhibits negligible temperature dependence and essentially remained at noise level.

IV. Conclusion

In this letter, we have demonstrated a SiNW-based TFET with a record low SS of 30 mV/decade at room temperature for low-voltage operation. An SS of 50 mV/decade is observed for almost three-decade change in drain current, and a high $I_{\mathrm{on}}/I_{\mathrm{off}}$ of five orders has been achieved. This work confirms TFET as a potential candidate for future low-power and energy-efficient electronics.

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