Compact Modeling and Analysis of Through-Si-Via-Induced Electrical Noise Coupling in Three-Dimensional ICs

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***Abstract*—Through-silicon vias (TSVs) in 3-D integrated circuits (ICs), which are used for connecting different active layers, introduce an important source of coupling noise arising from electrical coupling between TSVs and the active regions. This paper, for the first time, presents compact models based on a fully analytical approach for the electrical coupling from a TSV to the active regions for a comprehensive set of 3-D IC substrate technologies including those with and without the high-conductivity buried layer in dual-well bulk CMOS technology in the presence of V_{DD}/V_{SS} rails. The models can be used during design validation of emerging 3-D ICs. The compact physical models are verified against full-wave electromagnetic (EM) simulations. A comparative analysis of the magnitude of the EM coupling noise for different 3-D technology scenarios, including both dual-well bulk CMOS and partially depleted silicon-on-insulator, is also presented. The compact models presented for dual-well bulk CMOS are subsequently employed for estimating the stay-away radius (safe distance) from the center of the TSVs to the active regions to minimize the impact of such coupling noise. In order to highlight the significance of the TSV to active-region EM coupling noise, a comparison is also made with the white noise in the active region and the flicker noise from the interface between the TSV oxide and silicon.**

***Index Terms*—Active region, coupling coefficient, noise, through-silicon via (TSV), 3-D integrated circuit (IC).**

I. Introduction

THREE-DIMENSIONAL integrated circuits (ICs) can provide reduced interconnect delay and a platform to integrate dissimilar technologies (e.g., digital, analog, RF circuits, etc.) on different active layers [1], [2]. High-aspect-ratio vertical interconnects, which are called through-silicon vias (TSVs), providing connectivity between layers constitute a key technology for 3-D ICs [3], [4]. While the TSVs themselves have been investigated from both fabrication [5]–[7] and simulation/modeling perspectives [3], [4], [8], [9], there is a need to investigate the impact of TSVs on other components in the 3-D IC system, such as the coupling noise from TSVs to the active region [10]. This is because the electrical noise coupling from the TSVs to the body voltage of MOSFET devices (which can change the threshold voltage) is crucial for analog and low-noise-tolerant circuits. A typical range of the noise coupling from fast-switching digital signals to noise-sensitive analog circuits is -35 to -80 dB [11].

The literature contains experimental [12] and some simulation-based approaches that address this problem. However, the simulation approaches have substantial limitations that we address in this paper. The coupling noise generated by a typical TSV is studied in [13], but the simulation is based on a 2-D approximation, which is not accurate. The noise coupling from active devices to a TSV is discussed in [14], whereas the coupling from TSVs to active devices is studied in [15]. However, [13]–[15] have oversimplified the simulated structure: the body resistivity of n-channel MOSFETs (NMOSFETs) has been assumed to be the same value as that of the bulk p-type substrate. Note that practical configurations used in advanced bulk CMOS technology employ dual-well structures, where both n-well and p-well are required and the resistivity in the p-well is far smaller than that in the bulk regions [16]. In addition, the capacitance contribution from the silicon depletion region surrounding the TSV isolation oxide, which has not been included in [14] and [15], is essential to the TSV admittance/impedance estimation [3], [4], [8], [9] and is necessary for accurately determining any coupling noise.

II. TSV Configuration in Different Types of 3-D Technologies

There are various types of configurations in 3-D technologies including face-to-face and face-to-back bonding, wafer-to-wafer and die-to-wafer bonding, TSV first and TSV last, etc. [5]–[7]. The common aspect of all these configurations is the TSV, which is a high-aspect-ratio cylindrical metal punching through but isolated from the Si substrate (see Fig. 1). On the other hand, there are various Si-substrate configurations in state-of-the-art CMOS technologies including bulk CMOS and SOI technologies. A dual-well (having both p-well and n-well on the p-type substrate) configuration is the most typical structure in bulk CMOS technologies [see Fig. 1(a) and (b)]. To

Manuscript received February 27, 2011; revised July 16, 2011; accepted August 15, 2011. Date of current version October 21, 2011. This work was supported in part by the National Science Foundation under Grant CCF-0917385 and in part by UC Discovery under Grant COM09S-156729. The review of this paper was arranged by Editor Z. Celik-Butler.

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Digital Object Identifier 10.1109/TED.2011.2166156

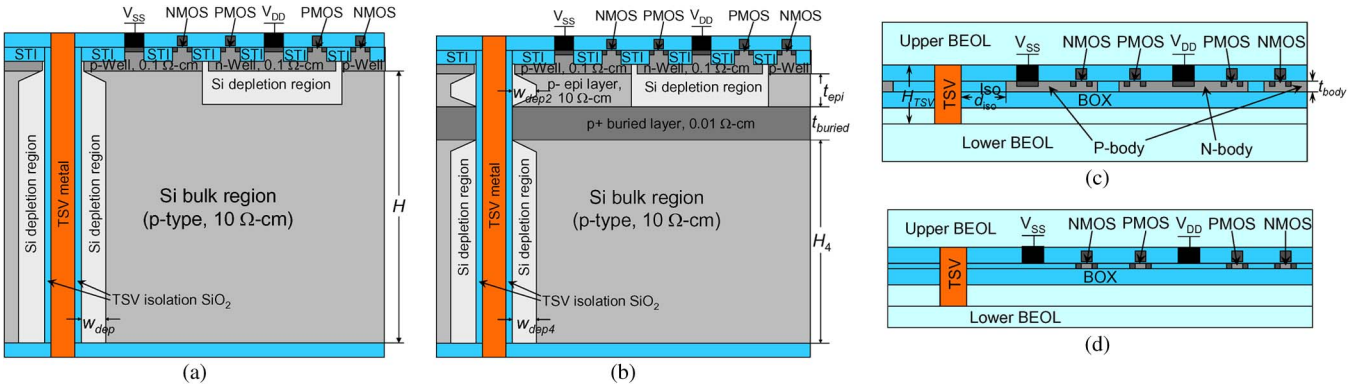

Fig. 1. Cross-sectional view of TSVs in different CMOS technologies (at the upper layer of a 3-D IC), including (a) bulk CMOS without a p+ buried layer (also valid for FD-SOI on thin BOX), (b) bulk CMOS with a p+ buried layer, (c) PD-SOI with body contacts, and (d) conventional FD-SOI (also valid for FinFETs). BEOL refers to back-end-of-line, for the upper and lower active layers. All of (a), (b), (c), and (d) assume a face-to-back configuration.

suppress latch-up, the substrate can contain a low-resistivity p+ buried layer [see Fig. 1(b)] [16], whose presence, however, can induce substantial substrate eddy-current losses at high frequencies [17] and thereby be harmful to on-chip inductors. TSVs in SOI technologies can be quite different from those in bulk CMOS technologies: the buried oxide (BOX) layer is a good etch stop; thereby, the thickness of the overlying silicon layer can be much thinner [18]. SOI technologies can be broadly classified as partially depleted (PD) SOI, fully depleted (FD) SOI, and FinFET (a Fin-based, multigate Field Effect Transistor) technologies. In low-noise applications, PD-SOI can have a body contact, which is similar to the bulk CMOS [see Fig. 1(c)]. There are two types of FD-SOI, i.e., the conventional FD-SOI and the FD-SOI on thin BOX (on the order of 10 nm) [19], [20]. The conventional FD-SOI and the FinFET do not have body contacts [see Fig. 1(d)], which is unlike other technologies, and will not be quantitatively discussed in this paper. Qualitatively, the coupling noise of the TSV to the active regions in FinFETs is likely to be much smaller since the body is well shielded by the gate, but the importance of the TSV coupling noise on the conventional FD-SOI is unclear. On the other hand, the FD-SOI on the thin BOX, which uses the silicon substrate as the fourth terminal of the MOSFET, shows many advantages over the conventional FD-SOI, such as suppressed drain-induced barrier lowering, better isolation between MOSFETs, and compatibility with bulk CMOS. From a TSV point of view, the FD-SOI on the thin BOX is similar to the bulk CMOS technologies than to the SOI technologies, in the sense that it also needs the dual well as body contacts ([see Fig. 1(a)]), with the exception that there is an ultrathin BOX below the active devices. Consequently, the simulation and modeling of TSV coupling noise to the body of the active region for the case of bulk CMOS is also valid for the case of the FD-SOI on the thin BOX.

III. Coupling Noise of TSV to the Body of Bulk CMOS

In this paper, to analyze the high-frequency characteristics of the TSV structures, we use a full-wave electromagnetic (EM) simulation tool (high frequency structure simulator, HFSS [23]) as a standard, and we develop quasi-electrostatic analytical models.

One may ask the validity of using pure EM simulation and modeling in analyzing a semiconductor-based problem. It is true that the pure EM simulation and modeling cannot include the semiconductor physics (drift, diffusion, generation, recombination, emission, etc.). However, as is illustrated in the Appendix, as long as the dc current is zero or negligibly small, we can still use the pure EM simulation or modeling to analyze the high-frequency small-signal ac characteristics, once the depletion region boundary is properly defined (the conductivity is set to zero within the depletion region boundary, whereas the conductivity is set to the bulk value outside the boundary). For example, as shown in the Appendix, after defining the depletion region boundary as the points where the carrier concentration equals half of the dopant concentration, we can use the pure quasi-electrostatic model to analyze p-n junctions in both zero- and reverse-bias conditions.

In our structures, the n-well-to-p-substrate junctions are always under reverse bias, whereas the TSV to p-substrate is a MOS structure. Therefore, once the depletion region boundary is properly defined, it is valid to use pure EM simulation or modeling to analyze the high-frequency small-signal ac characteristics. The depletion region boundary can be obtained by either a semiconductor simulation tool (such as Silvaco ATLAS [25], as in Fig. 2) or by using the equations derived in [3], [4].[1] After defining the depletion region boundary, we can analyze the high-frequency characteristics of the structures we are interested in. The pure EM simulation has the benefit of solving linear equations, which is much more stable and easier to converge than the nonlinear coupled EM and semiconductor simulation.[2]

[1]The depletion region width needs to be calculated according to the TSV bias if the bias voltage of the TSV is between the flatband voltage and the threshold voltage. On the other hand, beyond certain amount of oxide charge and/or SiO_2-Si interface charge, the threshold voltage becomes negative, and the depletion width has the maximum value and independent of small bias voltage. Our general methodology is valid for both the cases once the depletion region is carefully extracted.

[2]The approach of using pure EM simulation after finding the depletion region boundaries can be found in prior works [3], [4], [8].

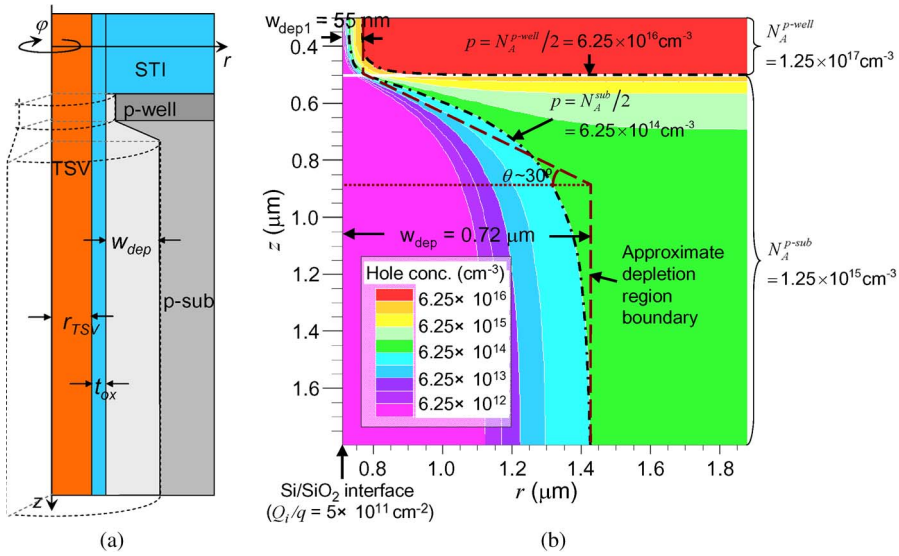

Fig. 2. (a) Schematic view of the approximate depletion region boundary, which can be obtained by finding (b) the distribution of hole concentration p (in z-r cross-section) from an electrostatic simulation tool (Silvaco ATLAS [25], 3-D cylindrical system simulation). The depletion region boundary is defined as the hole contour line where the hole concentration equals half the dopant concentration ($p = N_A/2$) (the dash-dot line), which can be approximated as the dash line. Rotating the dash line around the z-axis, the boundary in 3-D can be obtained [as shown in (a)]. In this plot, $r_{\rm TSV} = 0.59$ μm (from the ITRS 22-nm technology node, Year 2013 [26]), $t_{\rm ox} = 118$ nm, and other parameters and their values are shown in the plot.

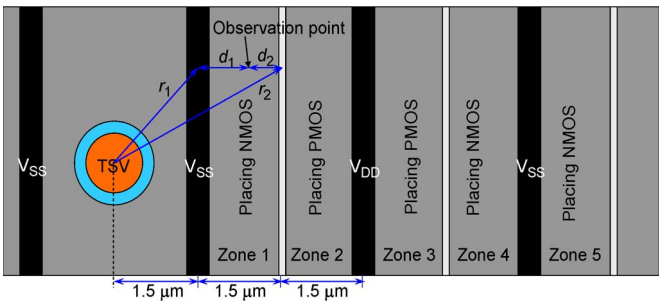

Fig. 3. Top-view schematic plot of a TSV in bulk CMOS technology. The center-to-center distance of $V_{\rm SS}$ to $V_{\rm DD}$ is 3 μm; the geometrical parameters d_1, d_2, r_1, r_2, and the zone indices (zones 1–5) are defined in the plot.

A. Bulk CMOS Without p+ Buried Layer

The high-frequency coupling from the TSV to an observation point (OP) at the silicon surface (see Fig. 3, i.e., a typical top view[3]) can be simulated using HFSS [23], as shown in Fig. 4. Here, both the $V_{\rm SS}$ and $V_{\rm DD}$ lines are the ac ground, and there is no outside current source connecting to the OP. The data labeled as "no inductive" are obtained by arbitrarily setting the permeability of all materials to be 0.01 times the vacuum permeability. The data labeled as "no p-wells" are obtained by eliminating the p-wells. Note that the inductive coupling is actually negligible (since artificially changing the permeability of all the materials has a negligible impact on the results). Hence, in the following analysis, all the analytical approaches need not consider the inductive coupling.[4] On the other hand, the dual-well configuration, which is not considered in [13]–[15], turns out to be a very important factor affecting the coupling coefficient g_{21}. In other words, eliminating p-wells or assuming an n-well-only configuration will result in significant errors (i.e., can be as large as several tens of decibels).[5]

The noise in the body of active devices can be coupled to the device performance through the body effect, which can be expressed as the relation between the threshold voltage $V_{\rm th}$ and the body voltage $V_{\rm BS}$: for the NMOSFET

$$V_{\rm th} = V_{\rm th0} + \gamma\left(\sqrt{2\phi_F - V_{\rm BS}} - \sqrt{2\phi_F}\right) \approx V_{\rm th0} - \frac{\gamma}{2\sqrt{2\phi_F}} \cdot V_{\rm BS} \quad (1)$$

where $V_{\rm th0}$ is the threshold voltage at zero body voltage, γ is the body-effect parameter, and $2\phi_F$ is the surface-potential parameter. According to the predictive technology model [27], the body doping concentration at the depletion region boundary between the channel and the body in a 22-nm technology node is 5.5×10^{18} cm^{-3}, which implies that $\gamma = 0.414$ V$^{1/2}$ and $2\phi_F = 1.02$ V. In such a situation, the $V_{\rm th}$ variation of NMOSFET is equal to $0.205|g_{21}|$ times the voltage variation of TSVs.

The analytical estimation of the coupling noise from the TSV to the body in bulk CMOS (without the p+ buried layer) is derived from an equivalent RC network [see Fig. 5(a)] and a uniform line-current-source approximation [see Fig. 5(b)]. The TSV self-impedance Z_{11} is the series combination of the MOS

[3]The placement of $V_{\rm SS}$ and $V_{\rm DD}$ lines as periodical power rails is one of the most common layout structures [21]. This placement implies that the $V_{\rm DD}$ and $V_{\rm SS}$ (ac grounds) are distributed everywhere in a very large scale integration chip and serves as local references to the active regions. A reasonable assumption is to place each signal TSV in the center between two power lines (as in [22, Fig. 6(a)]). Note that the ratio of the TSV diameter to the distance between power lines in [22] is assumed to be much larger that that in this paper. Therefore, each signal TSV in [22] has to break one power line, but each signal TSV in this paper can fit in between two neighboring power lines.

[4]Since the inductive coupling is negligible, a quasi-electrostatic solver (such as Maxwell 3-D [24]) is good enough to handle the analysis. However, in the subsequent analysis, we still use HFSS and the actual permeability, which is a bit of an overkill. We neglect the inductive coupling for analytical models.

[5]"p-wells" have much higher conductivity than the substrate. Therefore, when having the same level of noise current injection, the induced noise voltage is much lower.

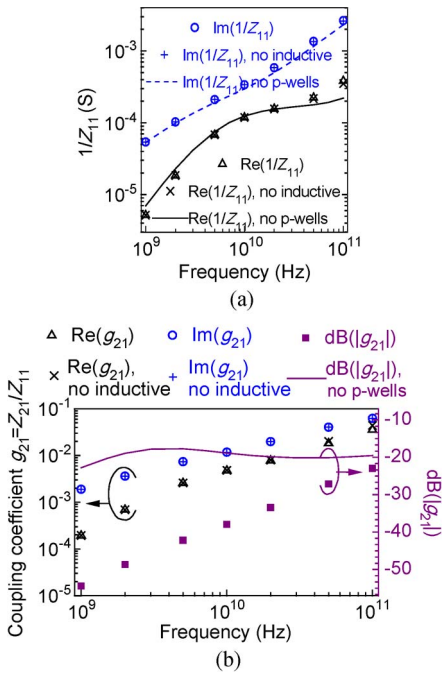

Fig. 4. HFSS simulation of bulk CMOS without the buried p+ layer. (a) $1/Z_{11}$ indicates the current injected into the TSV divided by the TSV voltage. (b) g_{21} indicates the voltage of OP divided by the TSV voltage. Parameters: bulk conductivity $\sigma_{\rm sub} = 10$ S/m; well conductivity $\sigma_{\rm well} = 10^3$ S/m; OP in zone 1 (see Fig. 3); $d_1 = 1\ \mu$m; $d_2 = 0.5\ \mu$m; $r_1 = 1.5\ \mu$m; $r_2 = 3\ \mu$m; $t_{\rm well} = 0.5\ \mu$m; $t_{\rm STI} = 0.3\ \mu$m; $w_{\rm ct} = 0.4\ \mu$m; $H = 14.5\ \mu$m; $r_{\rm TSV} = 0.59\ \mu$m; $t_{\rm ox} = 118$ nm; $w_{\rm dep} = 0.72\ \mu$m (the definition of the geometrical parameters can be found in Figs. 3 and 5). The HFSS setup is described as follows: the ac ground lines ($V_{\rm SS}$ and $V_{\rm DD}$) are made of metal with an equivalent conductivity of 1.8×10^7 S/m, and they are physically connected roughly 45 μm away from the TSV. Port 1 is between the TSV top and the nearest point in the nearest right-hand-side $V_{\rm SS}$ line. Port 2 is between the OP and the nearest point in the nearest $V_{\rm SS}$ line. The same setup is valid for every HFSS simulations in the following figures.

(oxide and depletion region) capacitance C_1, as well as the admittance due to the conductive and capacitive substrate Y_2, as follows:

$$Z_{11} \approx (j\omega C_1)^{-1} + Y_2^{-1} \tag{2}$$

where ω is the radial frequency. C_1 can be expressed as

$$\begin{aligned}\frac{1}{C_1} &= \frac{1}{2\pi H\varepsilon_{\rm ox}} \cdot \ln\left(\frac{r_{\rm TSV}+t_{\rm ox}}{r_{\rm TSV}}\right) + \frac{1}{2\pi H\varepsilon_{\rm Si}} \\ &\quad \cdot \ln\left(\frac{r_{\rm TSV}+t_{\rm ox}+w_{\rm dep}}{r_{\rm TSV}+t_{\rm ox}}\right) \\ &= 1/C_{1,\rm function}(H, r_{\rm TSV}, t_{\rm ox}, w_{\rm dep})\end{aligned} \tag{3}$$

where H is the substrate height; $\varepsilon_{\rm si}$ and $\varepsilon_{\rm ox}$ are the permittivity of Si and SiO_2, respectively; $r_{\rm TSV}$ is the radius of the TSV metal; $t_{\rm ox}$ is the thickness of the TSV isolation oxide; $w_{\rm dep}$ is the width of the depletion region surrounding the TSV isolation oxide; and $C_{1,\rm function}$ (i.e., a function of H, $r_{\rm TSV}$, $t_{\rm ox}$, and $w_{\rm dep}$) is defined from the expression in (3), which will be used in the following subsections. From the uniform line-current-source approximation, the OP voltage along the depletion region boundary can be expressed as shown at the bottom of the page, where I is the total current entering the TSV; $r_0 = r_{\rm TSV} + t_{\rm ox} + w_{\rm dep}$ is the radius of the TSV depletion region boundary; z is the vertical coordinate [defined in Fig. 5(b)] of the OP; $\sigma_{\rm sub}$ is the conductivity of the Si substrate; z' is the vertical coordinate of the current source along the z-axis (the center of the TSV); and the integration indicates that the OP voltage $V(r_0, z)$ is due to the current injection from all the sources. The terms $1/\sqrt{r_0^2 + (z-z')^2}$ and $1/\sqrt{r_0^2 + (z+z')^2}$ in (4) are the Green's function of the point current source (similar to point charge) at (0, z) and its image at (0, z'), respectively. By averaging $V(r_0, z)$

$$\begin{aligned}\frac{1}{Y_2} &\approx \frac{\overline{V(r_0,z)}}{I} = \frac{1}{H}\int_0^H \frac{V(r_0,z)}{I}dz \\ &\approx \frac{2\ln\left(\frac{H}{r_0}\right) - 2 + \frac{3r_0}{H}}{4\pi H(\sigma_{\rm sub} + j\omega\varepsilon_{\rm Si})} (H \gg r_0).\end{aligned} \tag{5}$$

This expression[6] is singular at $H \to 0$. To make it normal for small H, one can define a segmental function as follows:

$$f_1(r_0, H) = \begin{cases} \frac{2\pi H}{\ln(H/r_0) - 1 + 1.5r_0/H}, & H > 3r_0 \\ 26.30r_0 + 1.729H, & H \le 3r_0 \end{cases} \tag{6}$$

which is plotted in Fig. 5(c). Obviously, both $f_1(r_0, H)$ and its first-order derivative are continuous, i.e., with no singular behavior. Y_2 can then be derived as

$$Y_2 = (\sigma_{\rm sub} + j\omega\varepsilon_{\rm Si}) f_1(r_0, H). \tag{7}$$

In addition, from the approximation, the current density injecting into the wells $J(r, 0)$, which has a direction of $-\hat{z}$, can be expressed as

$$J(r,0) = (\sigma_{\rm sub} + j\omega\varepsilon_{\rm Si}) \left.\frac{\partial V}{\partial z}\right|_{z=0} = I \cdot f_2(H, r) \tag{8}$$

[6]Using an uniform line current source and a lumped value instead of distributed "Y_2" is an approximation, which is obviously valid when the impedance of the TSV isolation dielectric and depletion region ($|1/j\omega C_1|$) is much greater than $|1/Y_2|$. However, what we found from the simulation results shows that even if $|1/Y_2|$ has the same order or is greater than $|1/j\omega C_1|$, our approximation is still a reasonable estimation in terms of impedance extraction.

$$\begin{aligned}\frac{V(r_0,z)}{I} &= \frac{\int_0^H \left[1/\sqrt{r_0^2 + (z-z')^2} - 1/\sqrt{r_0^2 + (z+z')^2}\right] dz'}{4\pi H \cdot (\sigma_{\rm sub} + j\omega\varepsilon_{\rm Si})} \\ &= \frac{2\text{arcsinh}(z/r_0) + \text{arcsinh}\left((H-z)/r_0\right) - \text{arcsinh}\left((H+z)/r_0\right)}{4\pi H \cdot (\sigma_{\rm sub} + j\omega\varepsilon_{\rm Si})}\end{aligned} \tag{4}$$

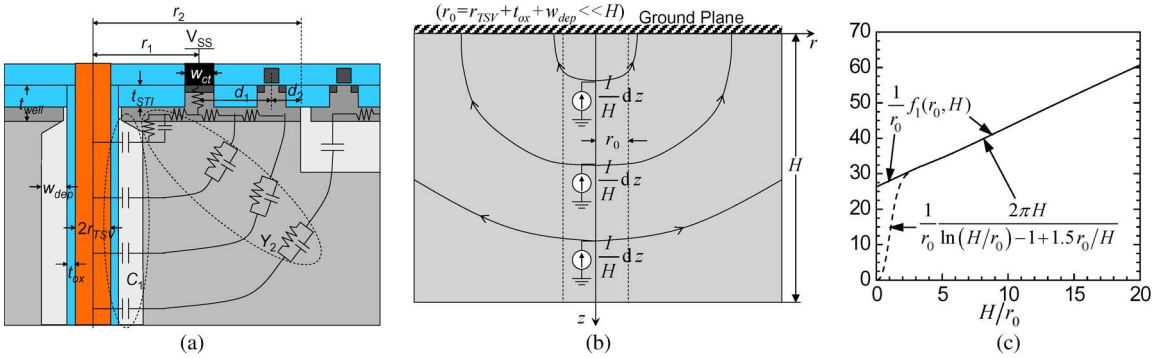

Fig. 5. From (a) equivalent RC network and (b) uniform line-current-source approximation (indicating that the current source is uniformly distributed along the line), the TSV self-impedance Z_{11} and the coupling coefficient g_{21} in the case of bulk CMOS without the p+ buried layer can be derived. H is the substrate height [see Fig. 1(a)]; I is the total current entering the TSV; the labeling d_1, d_2, r_1, r_2, $t_{\rm well}$, $t_{\rm STI}$, $w_{\rm ct}$, $r_{\rm TSV}$, $t_{\rm ox}$, and $w_{\rm dep}$ in (a) are consistent with previous figures. C_1 and Y_2 are defined in (2). (c) shows the curve of $f_1(r_0, H)$ [a function defined in (6)].

where function $f_2(H, r)$ is

$$f_2(H,r) = \frac{1}{2\pi H} \cdot \frac{\sqrt{r^2+H^2}-r}{r\sqrt{r^2+H^2}}. \tag{9}$$

Z_{21}, which is the mutual impedance between the TSV and the OP or the voltage at the OP divided by the total current from the TSV, can then be expressed as the total IR drop due to $J(r, 0)$ as follows:

$$Z_{21} \approx \frac{J(r_1,0)+J(r_2,0)}{2I} \cdot \left[\frac{d_1 d_2 + d_1^2/2}{(t_{\rm well}-t_{\rm STI})\sigma_{\rm well}} + \frac{2t_{\rm STI}}{w_{\rm ct}\sigma_{\rm well}} \cdot (d_1+d_2)\right] \tag{10}$$

where r_1 and r_2 are the horizontal distances from the TSV center to the two boundaries of the well, in which the OP lies; d_1 and d_2 are the horizontal distances from the OP to the two boundaries of the well; $t_{\rm well}$ and $t_{\rm STI}$ are the thicknesses of the well and the shallow-trench isolation (STI) region, respectively; $w_{\rm ct}$ is the width of the well contact; and $\sigma_{\rm well}$ is the conductivity of the well.[7] The geometrical parameters d_1, d_2, r_1, r_2, $t_{\rm well}$, $t_{\rm STI}$, $w_{\rm ct}$, $r_{\rm TSV}$, $t_{\rm ox}$, H, and $w_{\rm dep}$ are also labeled in Figs. 3 and 5. The coupling coefficient g_{21}, i.e., from the TSV to the OP, can then be expressed as $g_{21} = Z_{21}/Z_{11}$.

The calculation results of Z_{21} and g_{21} are compared with that of HFSS in Figs. 6 and 7 with various frequencies and distances to the TSV. Good agreement is achieved, except when the distance to the TSV is large and the frequency is low (for this situation, the coupling noise is negligible). The discrepancy arises from the fact that the current flowing into n-wells is suppressed, whereas that into p-wells is enhanced at lower frequency due to the high impedance of the depletion region between the n-wells and the p-substrate.

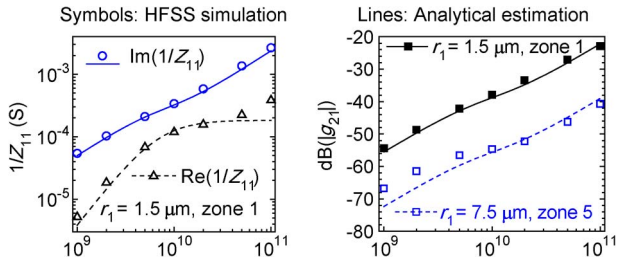

Fig. 6. HFSS simulation and analytical estimation results of (a) $1/Z_{11}$ and (b) dB($|g_{21}|$) in the bulk CMOS without the buried p+ layer as a function of frequency. All parameters are the same as in Fig. 4, except for the open squares and dash line in (b), where the OP is in zone 5, $r_1 = 7.5$ μm, and $r_2 = 9$ μm.

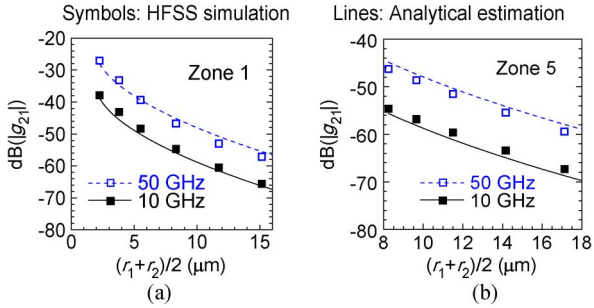

Fig. 7. HFSS simulation and analytical estimation results of coupling noise dB($|g_{21}|$) in bulk CMOS without the buried p+ layer as a function of horizontal distance from the TSV center to the OP in (a) zone 1 and (b) zone 5. r_1 and r_2 are defined in Fig. 3. All other geometrical and material parameters are the same as in Fig. 4.

B. Bulk CMOS With the p+ Buried Layer

In the presence of a low-resistivity p+ buried layer, the noise current can spread through it. Therefore, compared with the case without the p+ buried layer, the noise coupling from the TSV to nearby (far-away) active regions in the situation with the p+ buried layer is less (more). The noise coupling in this situation can be treated as the equivalent network of current

[7]The current density outside the wells is not affected by the property of the wells as long as the well conductivity is much greater than the substrate. In such situation, the current density outside the wells and the current density injected into the wells can be obtained from a ground plane approach, which explains the term of $[J(r_1,0)+J(r_2,0)]/2I$ in (10). Note that a distributed rather than a constant current injection in the region between r_1 and r_2 is a more accurate assumption. However, when $|r_2 - r_1| < r_1$, we can treat the current density injection as uniform $[J(r_1,0)+J(r_2,0)]/2$. Once the current injected into the wells is obtained, we can utilize the resistance network in the well to obtain the voltage drop of a particular position of a well w.r.t. the ground line, which explains the term in the second line of (10).

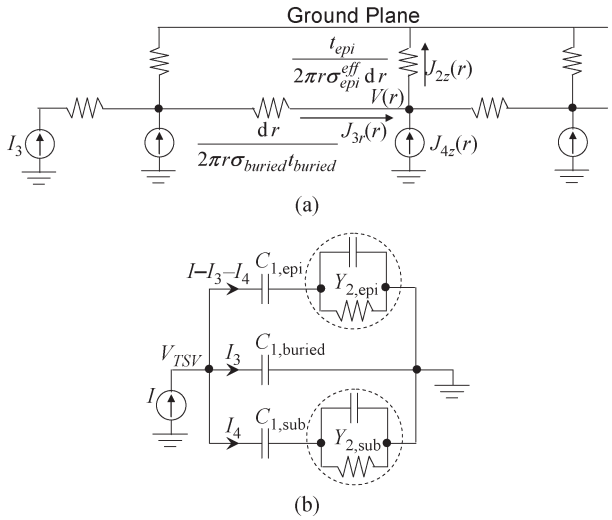

Fig. 8. (a) Equivalent network showing the noise-current spreading and (b) equivalent RC network for the extraction of the TSV self-impedance Z_{11} and the weight of different current components (I, I_3, and I_4) in the case of the bulk CMOS with the p+ buried layer. $t_{\rm buried}$, $t_{\rm epi}$, $\sigma_{\rm buried}$, $\sigma_{\rm epi}^{\rm eff}$, I, I_3, $J_{3r}(r)$, I_4, $J_{4z}(r)$, $J_{2z}(r)$, $V(r)$, $C_{1,\rm epi}$, $Y_{2,\rm epi}$, $C_{1,\rm buried}$, $C_{1,\rm sub}$, and $Y_{2,\rm sub}$ are defined in the text.

spreading through the p+ buried layer [see Fig. 8(a)]. The corresponding differential equations are

$$J_{3r}(r)/\sigma_{\rm buried} = -\frac{d}{dr}V(r) = -\frac{d}{dr}\left[J_{2z}(r)\cdot t_{\rm epi}/\sigma_{\rm epi}^{\rm eff}\right] \tag{11a}$$

$$\frac{d}{dr}[2\pi r t_{\rm buried}J_{3r}(r)] = 2\pi r\cdot[J_{4z}(r)-J_{2z}(r)]+I_3\delta(r) \tag{11b}$$

where $\sigma_{\rm buried}$ is the conductivity of the buried layer; $\sigma_{\rm epi}^{\rm eff} = \sigma_{\rm epi} + j\omega\varepsilon_{\rm Si}$ is the effective conductivity of the Si epilayer ($\sigma_{\rm epi}$ is the dc conductivity of the Si epilayer); $t_{\rm buried}$, $t_{\rm epi}$, and H_4 are the thicknesses of the buried layer, the Si epilayer, and the Si bulk region, respectively [$t_{\rm buried}$, $t_{\rm epi}$, and H_4 are schematically shown in Fig. 1(b)]; $\delta(r)$ is the delta function; I_3 is the current injected directly into the buried layer; $J_{3r}(r)$ is the horizontal current density in the buried layer (the dependence of $J_{3r}(r)$ on z is very weak and thereby can be ignored); $J_{4z}(r)$ is the vertical current density injected into the buried layer through the low-conductivity bulk (the total amount of $J_{4z}(r)$ is defined as I_4); $J_{2z}(r)$ is the vertical current density injected into the wells (ground plane) from I_3 and I_4 ($J_{2z}(r)$ can be approximately treated as the same as the vertical current density injected from the p+ buried layer); and $V(r)$ is the voltage in the p+ buried layer as a function of the radius from the TSV. Equation (11a) is essentially Ohm's law, which connects the current density with electric field; (11b) is essentially the Kirchhoff's current law, which indicates the continuity of the current density. Equations (11a) and (11b) result in

$$\frac{d}{dr}\left[2\pi r t_{\rm buried}\sigma_{\rm buried}\cdot t_{\rm epi}/\sigma_{\rm epi}^{\rm eff}\cdot\frac{d}{dr}J_{2z}(r)\right] = 2\pi r\cdot[J_{2z}(r)-J_{4z}(r)] - I_3\delta(r). \tag{12}$$

On the other hand, $J_{4z}(r)$ is similar with the situation in the low-conductivity substrate, which is discussed in Section III-A. Therefore, $J_{4z}(r)$ can be expressed as

$$J_{4z}(r) = I_4 f_2(H_4, r) \tag{13}$$

where function f_2 is predefined in (9). One can define the current-spreading parameter L_D (with a unit of length) as

$$L_D = \sqrt{t_{\rm buried}\sigma_{\rm buried}\cdot t_{\rm epi}/\sigma_{\rm epi}^{\rm eff}}. \tag{14}$$

When $|L_D| \gg H_4$

$$2\pi r J_{4z}(r) \to I_4\delta(r) \tag{15}$$

Then, an analytical expression for $J_{2z}(r)$ can be obtained as follows:

$$J_{2z}(r) = (I_3+I_4)\mathrm{K}_0(r/L_D)/\left(2\pi L_D^2\right) \tag{16}$$

where K_0 is the zeroth-order modified Bessel function of the second kind. Subsequently, the total current density injected into the wells $J(r)$ is expressed as the sum of two components as follows:

$$J(r) \approx J_{2z}(r) + (I-I_3-I_4)f_2(t_{\rm epi}, r) \tag{17}$$

where I is the total current and $I-I_3-I_4$ is the current injected into the well through the Si epilayer but not through the p+ buried layer. The weight of the current can be found from the impedance network [see Fig. 8(b)].

Here, $C_{1,\rm epi}$, $C_{1,\rm buried}$, and $C_{1,\rm sub}$ can be expressed as

$$\begin{cases} C_{1,\rm epi} = C_{1,\rm function}(t_{\rm epi}, r_{\rm TSV}, t_{\rm ox}, w_{\rm dep2}) \\ C_{1,\rm buried} = C_{1,\rm function}(t_{\rm buried}, r_{\rm TSV}, t_{\rm ox}, 0) \\ C_{1,\rm sub} = C_{1,\rm function}(H_4, r_{\rm TSV}, t_{\rm ox}, w_{\rm dep4}) \end{cases} \tag{18}$$

where $t_{\rm epi}$ and $t_{\rm buried}$ are the thicknesses of the low-conductivity p− epilayer and the high-conductivity p+ buried layer, respectively; H_4 is the thickness of the bulk p− Si substrate; $r_{\rm TSV}$ is the radius of the TSV metal; $t_{\rm ox}$ is the thickness of TSV isolation SiO_2; $w_{\rm dep2}$ and $w_{\rm dep4}$ are the width of the depletion region surrounding the TSV in the p− epilayer region and bulk p− Si substrate, respectively; and $C_{1,\rm function}$ is a function of geometrical parameters, as predefined in (3) [the geometrical parameters are schematically shown in Fig. 1(b)].

On the other hand, $Y_{2,\rm epi}$ and $Y_{2,\rm sub}$ can be expressed as

$$\begin{cases} Y_{2,\rm epi} = \sigma_{\rm epi}^{\rm eff}\cdot f_1(r_{\rm TSV}+t_{\rm ox}+w_{\rm dep2}, t_{\rm epi}) \\ Y_{2,\rm sub} = (\sigma_{\rm sub}+j\omega\varepsilon_{\rm Si})\cdot f_1(r_{\rm TSV}+t_{\rm ox}+w_{\rm dep4}, H_4) \end{cases} \tag{19}$$

where function f_1 is predefined in (6).

Using the impedance network in Fig. 8(b), (18), and (19), the TSV self-impedance Z_{11} and the weight of the current (I_3/I and I_4/I) can be obtained. Using (17), the total current density injected into the wells $J(r)$ can be obtained. The expression (10) for Z_{21} is a general expression, which is valid not only in Section III-A but also in this subsection. As a consequence, the coupling coefficient g_{21} can be obtained from $g_{21} = Z_{21}/Z_{11}$.

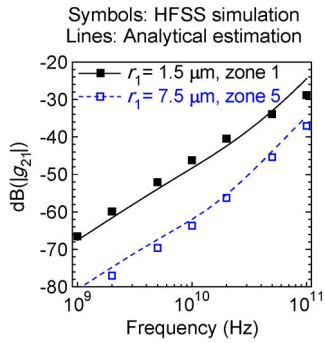

Fig. 9. HFSS simulation and analytical estimation results of the coupling noise dB($|g_{21}|$) in bulk CMOS with the buried p+ layer as a function of frequency. $t_{\rm buried} = 1$ μm. $t_{\rm epi} = 1$ μm. $H_4 = 12.5$ μm. $\sigma_{\rm epi} = \sigma_{\rm sub} =$ 10 S/m. $\sigma_{\rm buried} = 10^4$ S/m. $w_{\rm dep2} = w_{\rm dep4} = 0.72\mu$m (the definition of the parameters can be found in the text.

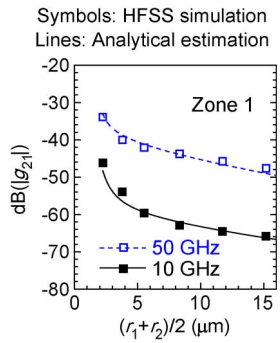

Fig. 10. HFSS simulation and analytical estimation results of the coupling noise dB($|g_{21}|$) in bulk CMOS with the buried p+ layer as a function of the horizontal distance from the TSV center to the OP in zone 1. r_1 and r_2 are defined in Fig. 3; other parameters are the same as in Fig. 9.

The results are compared with HFSS in Figs. 9 and 10 with various frequencies and distances to the TSV. Good agreement is obtained. Compared with the case without the p+ buried layer, the noise coupling from the TSV to nearby (far-away) active regions in the situation with the p+ buried layer is less (more). This is due to the noise spreading in the p+ buried layer.

IV. Coupling Noise of the TSV to the Body of PD-SOI

An accurate analytical estimation of coupling noise for PD-SOI substrates is difficult. This extra difficulty comes from two factors. First, the isolation region surrounding the TSV in the case of the SOI is essentially the isolation in the front-end-of-line (FEOL) process, which does not have an azimuthal symmetry (see the top view in Fig. 11). However, the one in bulk CMOS, which is essentially the TSV isolation dielectric, has an azimuthal symmetry (see the top view in Fig. 3). Second, the TSV aspect ratio in the case of the SOI is much smaller. Nonetheless, the noise coupling for the PD-SOI is much smaller than that of bulk CMOS, due to the significantly shorter TSV height, compared with that in bulk CMOS. The HFSS simulation results are shown in Figs. 12 and 13. The coupling noise values are roughly 10 to 40 dB lower than those in bulk CMOS.

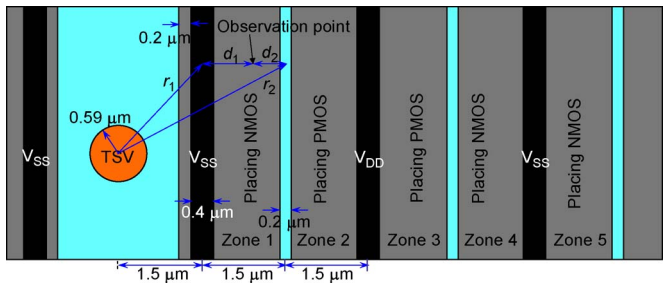

Fig. 11. Top-view schematic plot of the TSV in PD-SOI technology. The center-to-center distance of $V_{\rm SS}$ to $V_{\rm DD}$ is 3 μm; the geometrical parameters d_1, d_2, r_1, r_2 and the zone indices (Zone 1 to 5) are defined in the plot. Note that, in SOI technology, TSVs can be made through the isolation region, but in bulk CMOS, TSVs have to be isolated from the surrounding Si by thin isolation dielectric (SiO_2).

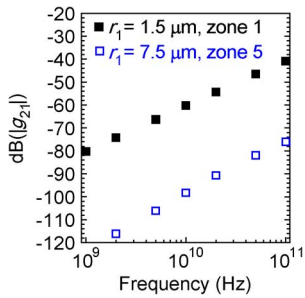

Fig. 12. HFSS simulation result of coupling noise dB($|g_{21}|$) in PD-SOI as a function of frequency. $t_{\rm body} = 60$ nm. $H_{\rm TSV} = 1.35$ μm. $d_1 = 1$ μm. $d_2 =$ 0.5 μm (the definition of the parameters can be found in Figs. 1(c) and 11). $\sigma_{p-{\rm body}} = 3 \times 10^3$ S/m. Other parameters are the same as in Fig. 11.

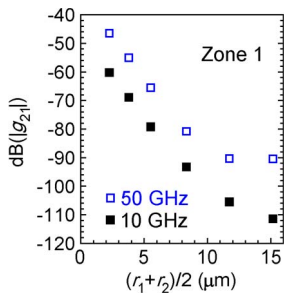

Fig. 13. HFSS simulation result of the coupling noise dB($|g_{21}|$) in PD-SOI as a function of the horizontal distance from the TSV center to the OP in zone 1. r_1 and r_2 are defined in Fig. 11; other parameters are the same as in Fig. 12.

V. Stay-Away Radius for Noise Coupling From TSVs

Depending on the circuit type (analog, RF, static logic, dynamic logic, etc.), the active devices can suffer different levels of noise coupling. The analytical TSV noise models can be used to estimate the stay-away (or safe) radius for different technology configurations. The stay-away radius is the minimum $(r_1 + r_2)/2$ that is allowed for a particular coupling coefficient at a particular frequency (r_1 and r_2 are defined in Fig. 3). In the 22-nm technology node, the significant frequency of the driver output signal is on the order of several tens of gigahertz [3], [4]. Therefore, we choose 50 GHz for the analysis. In Fig. 14(a), in the case of bulk CMOS without the p+ buried layer, the stay-away radius increases as the bulk Si conductivity increases, which is due to the decreasing TSV self-impedance. In Fig. 14(b), in the case of bulk CMOS with the p+

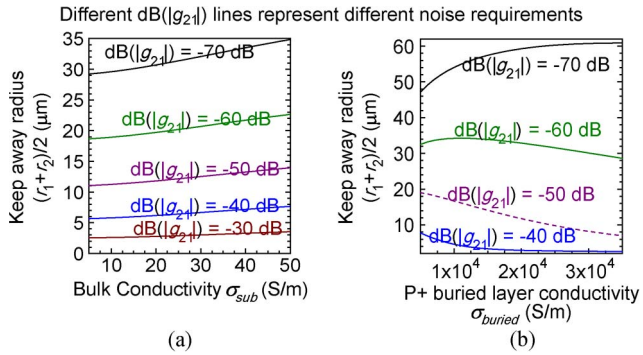

Fig. 14. Stay-away radius from analytical estimation results of the coupling noise dB($|g_{21}|$) in bulk CMOS (a) without the p+ buried layer as a function of $\sigma_{\rm sub}$ and (b) with p+ buried layer as a function of $\sigma_{\rm buried}$. OPs are in zone 1; frequency is 50 GHz; all parameters in (a), except $\sigma_{\rm sub}$ and $w_{\rm dep}$ (recalculated according to $\sigma_{\rm sub}$), are the same as in Fig. 7; all parameters in (b), except $\sigma_{\rm buried}$ are the same as in Fig. 10.

buried layer, the stay-away radius decreases (increases) as the conductivity of the p+ buried layer increases (increases) if the noise requirement is less (more) strict, which is due to greater current spreading.

VI. TSV Coupling-Noise Versus Other Noise Sources

The active devices suffer from many other kinds of noise, in addition to the coupling noise from the TSVs. In this section, we will discuss the impact of two kinds of noise, as compared with that from TSVs, i.e., the white (thermal) noise generated in the well and the flicker noise generated from the interface of TSV oxide and the Si substrate.

The white (thermal) noise originates from the thermal agitation of the charge carriers inside an electrical conductor (or semiconductor). The mean-square voltage variance per hertz of bandwidth $\overline{v_{\rm th}^2}$ of a resistor is given by the Johnson–Nyquist relation [28], [29] as follows:

$$\overline{v_{\rm th}^2} = 4k_BTR \tag{20}$$

where k_B is the Boltzmann constant, T is the temperature, and R is the resistance of the resistor.

We take the case of the bulk CMOS without the p+ buried layer as an example. To estimate the white noise voltage at the OP, we assume that the active region (where the OP lies) has a size of 1 μm in the direction parallel to the power rails and 0.4 μm in the direction vertical to the power rails, and the OP-to-power-rail-center distance $d_1 = 1$ μm (see Fig. 3). R can be obtained by the HFSS simulation, as defined in Section III-A, where $R \approx Z_{22}$, whereas Z_{22} is weakly dependent on frequency. From the simulation at 1 GHz, $R \approx Z_{22}$ is extracted as 2.17 kΩ. Therefore, at temperature of 300 K, $\sqrt{\overline{v_{\rm th}^2}} \approx 5.99\ {\rm nV}/\sqrt{\rm Hz}$.

To compare the contribution of the white noise and the TSV coupling noise to the active region, we apply a periodical trapezoidal voltage signal at the TSV, with a swing voltage of $V_{\rm swing} = 0.9$ V, a frequency of $f_{\rm clk} = 5$ GHz, a rise/fall time of 8 ps, and a pulsewidth (as when $V_{\rm TSV} = V_{\rm swing}$) of 92 ps. The signal can be expressed as a Fourier series given as

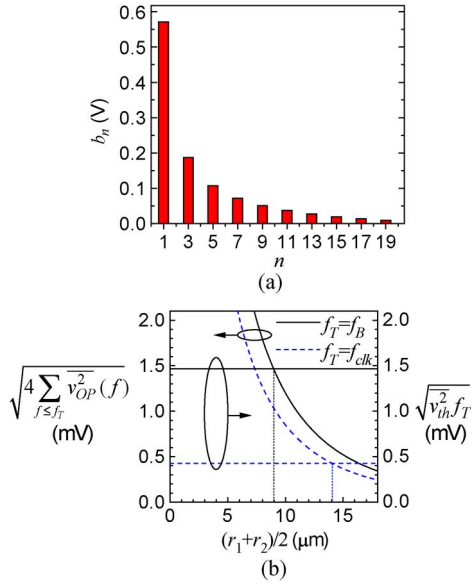

Fig. 15. (a) Coefficients of a Fourier series of a periodical trapezoidal voltage signal in (21), with a swing voltage of $V_{\rm swing} = 0.9$ V, a frequency of $f_{\rm clk} = 5$ GHz, a rise/fall time of 8 ps, and a pulsewidth (as when $V_{\rm TSV} = V_{\rm swing}$) of 92 ps. (b) When applying such voltage signal to the TSV, it will be coupled to the active region (averagely $(r_1 + r_2)/2$ from the TSV center) as coupling noise voltage. The coupling noise voltage to the active region as a result of four TSVs is compared with the white noise in the active region. r_1 and r_2 are defined in Fig. 3, the OP is in zone 1, and all other geometrical and material parameters are the same as in Fig. 4.

$$V_{\rm TSV}(t) = \frac{V_{\rm swing}}{2} + \sum_{n=1}^{\infty} b_n \sin(n \cdot 2\pi f_{\rm clk} \cdot t) \tag{21}$$

where b_n is the spectral voltage at each frequency and t is the time. In our situation, it is obvious that, when n is an even number, b_n must be zero. When n is odd, b_n can be plotted in Fig. 15(a). The mean-square voltage at each frequency of $nf_{\rm clk}$ at the TSV is then $b_n^2/2$. We consider the cutoff frequency f_T, i.e., above which the noise is not important. The summation of the mean-square voltage at the OP in the active region at all the frequencies below f_T gives $\sum_{f\le f_T} \overline{v_{\rm OP}^2}(f)$ (the total mean-square voltage at OP with frequencies below f_T). Obviously

$$\sum_{f\le f_T} \overline{v_{\rm OP}^2}(f) = \sum_{n}^{{\rm nf}_{\rm clk}\le f_T} \frac{1}{2}\left(b_n g_{21}(nf_{\rm clk})\right)^2 \tag{22}$$

where $g_{21}(f)$ is the voltage coupling coefficient from the TSV to the OP as a function of frequency f. Therefore, from (22) and the analytical model in Section III-A, we can obtain $\sqrt{4\sum_{f\le f_T} \overline{v_{\rm OP}^2}(f)}$, which is shown in Fig. 15(b) as a function of $(r_1 + r_2)/2$ (r_1 and r_2 are defined in Fig. 3; $(r_1 + r_2)/2$ denotes the average distance from TSV center to the active region). Note that the factor of 4 is from the assumption that the OP can be surrounded by approximately four signal TSVs with the same distance. Fig. 15(b) also shows the characteristic

distance of $(r_1 + r_2)/2$ that the TSV-to-active-region coupling noise $\sqrt{4\sum_{f\le f_T}\overline{v_{\rm OP}^2}(f)}$ is comparable with the white noise $\sqrt{\overline{v_{\rm th}^2}f_T}$ in the active region. For $f_T = f_{\rm clk} = 5$ GHz, the characteristic distance is calculated as 9 μm. For $f_T = f_B = 60$ GHz (f_B is the significant frequency determined by the digital signal rise/fall time; 60 GHz is a typical value in the driver–receiver circuit, as obtained in [4]), the characteristic distance is calculated as 14.1 μm.

The flicker noise is generated from the interface of the TSV oxide and the Si substrate. Due to the large interface state density at the interface of the TSV oxide and the Si substrate, one may wonder about the importance of the flicker noise. According to [30], the mean-square current per hertz of bandwidth per unit interface area $\overline{i_p^2}$ of the flicker noise can be expressed as

$$\overline{i_p^2} = 4k_BTG_p \tag{23}$$

where G_p is the total conductance per unit interface area due to the interface states. G_p can be expressed as

$$G_p(f) = \frac{1}{2}\cdot\frac{q^2N_{\rm ss}}{\sqrt{2\pi s_{\rm us}^2}}\cdot\int_{-\infty}^{\infty}\exp\left(-\frac{(u_s-\overline{u_s})}{2s_{\rm us}^2}\right)\cdot\frac{\ln\left(1+\omega^2\tau_m^2(u_s)\right)}{\tau_m(u_s)}du_s \tag{24}$$

where q is the elementary charge; $N_{\rm ss}$ is the interface state density; u_s and $\overline{u_s}$ are the possible surface potential and the mean surface potential in units of k_BT/q, respectively; $s_{\rm us}$ is the standard deviation of the surface potential; ω is the radian frequency ($\omega = 2\pi f$); and $\tau_m(u_s)$ is the hole capture time as a function of u_s. $\tau_m(u_s)$ can be expressed as

$$\tau_m(u_s) = \left(c_pN_a\exp(-u_s)\right)^{-1} \tag{25}$$

where c_p is the hole capture probability, N_a is the acceptor concentration, and $N_a\exp(-u_s)$ is the hole concentration at the surface.

Once $\overline{i_p^2}$ is obtained, the mean-square noise voltage at the OP in the active region can be expressed as

$$\overline{v_{\rm fk}^2}(f) = 2\pi(r_{\rm TSV}+t_{\rm ox})H\overline{i_p^2}Z_{21}^2 \tag{26}$$

where $r_{\rm TSV}$, $t_{\rm ox}$, H, and Z_{21} are defined in Section III.

We can evaluate the flicker noise from (23)–(25) and some reasonable assumptions of several parameters: we assume a typical fixed oxide charge density of 3.5×10^{11} cm^{-2} and a typical interface state density of $N_{\rm ss} = 5\times10^{11}$ cm^{-2} eV^{-1} (according to the experimental data of [9]), we assume $s_{\rm us} = 2.6$ and $c_p = 2.2\times10^{-9}$ cm^3/s (according to the data of [30]), and we also assume the geometrical and material information to be the same as that in Fig. 4. The flicker-noise voltage spectrum can then be obtained, as shown in Fig. 16(a). Note that the result does not show a $1/f^\alpha$ ($\alpha \ge 1$) behavior, as discussed in [30]. This is due to the fact that [30] considers the noise voltage across the depletion region, whose impedance is capacitive and proportional to $1/f$, whereas we consider the noise voltage in the p-wells, whose impedance is nearly independent of f. The total flicker-noise voltage below certain frequency as a function of bias voltage is shown in Fig. 16(b). Compared with Fig. 15(b), it can be concluded that the flicker noise is far less important than both the white noise in the well and the electrical coupling noise from the TSVs.

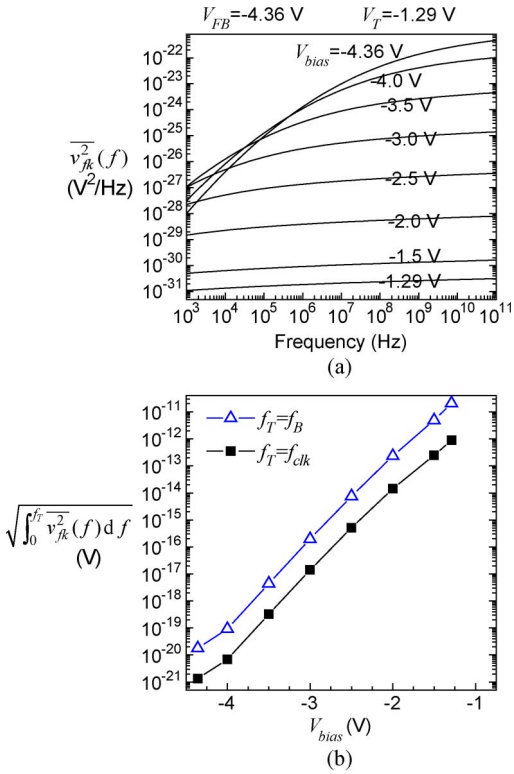

Fig. 16. (a) the mean-square flicker-noise voltage at OP in the active region $\overline{v_{\rm fk}^2}$ as a function of frequency and TSV bias voltage $V_{\rm bias}$. (b) the total flicker-noise root-mean-square voltage $\sqrt{\int_0^{f_T}\overline{v_{\rm fk}^2}(f)df}$ as a function of $V_{\rm bias}$. All geometrical and material parameters (except $w_{\rm dep}$, which depends on $V_{\rm bias}$) are the same as those in Fig. 4. $f_{\rm clk} = 5$ GHz, and $f_B = 60$ GHz. The flatband voltage $V_{\rm FB} = -4.36$ V and the threshold voltage $V_T = -1.29$ V are calculated by assuming $N_{\rm ss} = 5\times10^{11}$ cm^{-2} eV^{-1} and a fixed oxide charge density of 3.5×10^{11} cm^{-2}.

VII. Summary

A comprehensive treatment of EM coupling noise from TSVs to active regions in various 3-D IC technologies is presented with consideration of different active-layer scenarios, including the dual-well and high-conductivity buried layer in bulk CMOS technology, as well as the short TSV height and thin silicon layer thickness in SOI technology. Compact physical models for the bulk CMOS case are developed and verified against full-wave EM simulations. The compact models can be used to analyze the stay-away radius for robust layout designs in emerging 3-D ICs. An extended analysis of the white noise in the active region and the flicker noise from the interface between TSV oxide and silicon shows the importance of different kinds of noise: below certain distance from the TSV to the active region, the white noise in the active region is less important than the EM coupling noise from the TSV to the active region, whereas

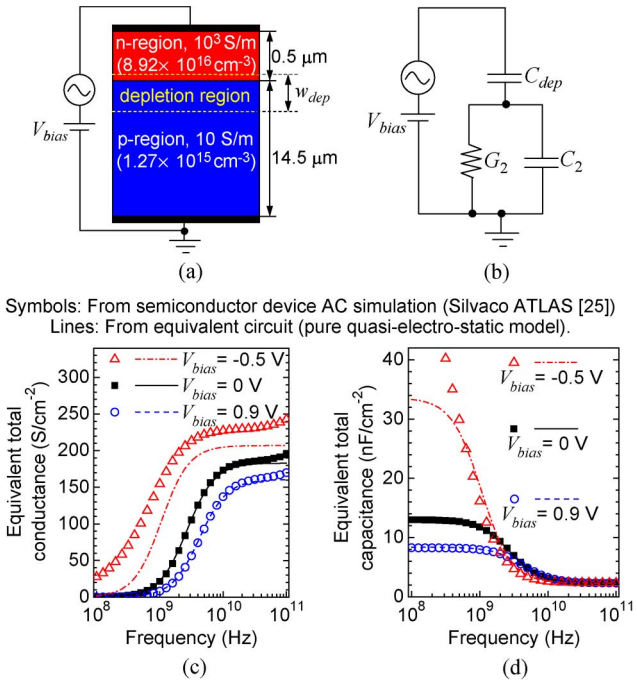

Fig. 17. High-frequency small-signal ac characteristics of a simple 1-D p-n junction. (a) Schematic plot. (b) Equivalent circuit (pure quasi-electrostatic model). (c) Equivalent total conductance. (d) Equivalent total capacitance. To obtain the parameters in the equivalent circuit in (b), the depletion region width $(w_{\rm dep})$ needs to be obtained. Here, we define the depletion region boundaries as where the carrier concentration equals the half of dopant concentration, which can be obtained from the semiconductor device dc simulation

the flicker noise from the interface between the TSV oxide and the silicon substrate is far less significant.

APPENDIX
VALIDITY OF PURE EM SIMULATION/MODELING

Here, we take a simple 1-D p-n junction as an example to explain the validity condition of using pure EM simulation or modeling on the high-frequency small-signal ac characteristics of semiconductor-based problems, once the depletion region boundary is properly defined (the conductivity is set to zero within the depletion region boundary, whereas the conductivity is set to the bulk value outside the boundary). The schematic plot and the equivalent circuit (pure quasi-electrostatic model) are shown in Fig. 17(a) and (b), whereas the results of high-frequency small-signal ac characteristics are obtained from both the semiconductor device simulation (Silvaco ATLAS [25]) and the equivalent circuit (pure quasi-electrostatic model).

We observe that the pure quasi-electrostatic model to analyze a p-n junction agrees with the semiconductor device ac simulation in both the zero-bias and reverse-bias $(V_{\rm bias} = 0.9\ {\rm V})$ conditions. On the other hand, the pure quasi-electrostatic model in the forward-bias condition $(V_{\rm bias} = -0.5\ {\rm V})$ disagrees with the semiconductor-device ac simulation. The reason behind the disagreement comes from the large diffusion current from minority carriers in a forward-bias p-n junction, which contributes to both conductance and capacitance (diffusion capacitance in parallel with depletion capacitance).

Fortunately, the pure EM simulation or modeling is valid for analyzing the high-frequency small-signal ac characteristics in the structures in this paper. This is because, in our structures, the n-well-to-p-substrate junctions are always under reverse bias, whereas the TSV to p-substrate is a MOS structure, which indicates zero or negligibly small dc current.

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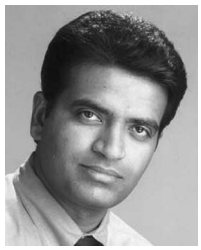

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