Scaling the Si MOSFET: From Bulk to SOI to Bulk

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Abstract—**Scaling the Si MOSFET is revisited. Requirements on subthreshold leakage control force conventional scaling to use high doping as the device dimension penetrates into the deep-submicrometer regime, leading to undesirable large junction capacitance and degraded mobility. By studying the scaling of fully depleted SOI devices, we note the important concept of controlling horizontal leakage through vertical structures. Several structural variations of conventional SOI structures are discussed in terms of a natural length scale to guide the design. The concept of *Vertical Doping Engineering* can also be realized in bulk Si to obtain good subthreshold characteristics without large junction capacitance or heavy channel doping.**

I. Introduction

OVER THE past thirty years, the primary challenge of VLSI has been the integration of an ever increasing number of devices with high yield and reliability. However, as device dimensions penetrate into the deep-submicrometer regime, the characteristics of a conventional MOSFET approach that of a resistor [1]. This difficulty is traditionally solved by increasing the threshold voltage through increased channel doping. At the same time, reliability constraints have led to reductions in the power supply voltage. The combination of high channel doping and capacitance, increased threshold voltage, and reduced supply voltage, imposes severe tradeoffs between standby power and circuit speed.

Brews' empirical scaling rule [2] has provided a successful guideline for the design of the conventional MOSFET. We begin by outlining the implications of the rule in the deep-submicrometer regime, and show how fully depleted SOI (silicon-on-insulator) structures attempt to circumvent the limitations faced by conventional deep-submicrometer devices. We then show that the innovative, but realistic device structures in bulk Si can mimic the SOI philosophy, providing well-behaved devices in the deep-submicrometer regime. Throughout the paper emphasis is placed on the fundamental concepts that govern the operation of such devices. To this end, we provide an analytic framework [3], within which scaling may be naturally understood, supporting the analytic treatment with two-dimensional (2D) numerical simulations [4], [5][1] where appropriate. What emerges from our analysis is a natural length scale, which may be used to predict the performance of a class of device structures both in bulk Si and SOI. We conclude by describing a particular device structure which may realize the promise of a well-behaved, deep-submicrometer device operating at room temperature.

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[1]Monte Carlo simulations are required to predict the device performance in the turn-on regime [5].

II. Direct Scaling

Various device scaling rules have been proposed [2], [6], [7]. Brews' empirical rule [2] provides a general guideline for the subthreshold region, and is considered the basic guideline for applications such as dynamic and static memory circuits, where leakage currents in the off state of the devices are important. The intrinsic device parameters for an NMOSFET are L_{eff}, t_{ox}, t_j, and V_{DD} (Fig. 1). (The symbols are defined in Table I.) According to Brews' formula, the effective channel length L_{eff} must be larger than L_{min} in order to achieve good subthresold behavior

$$L_{\text{min}} = A[t_j t_{\text{ox}}(w_s + w_d)^2]^{1/3} \tag{1}$$

where $A = 0.41$ Å $^{-1/3}$. Assuming that the device structure (defined by L_{eff}, t_{ox}, t_j, and V_{DD}) is fixed by technology and circuit requirements, and the designer is free only to vary the channel doping N_A, (1) can be reformulated in the following way to relate the channel doping to the intrinsic device parameters:

$$N_A \geq 1.8 \times 10^{17}\ \text{cm}^{-3}\ \frac{[\sqrt{V_{bi}} + \sqrt{V_{bi} + V_{DD}}]^2}{\text{volts}} \cdot \frac{t_j}{500\ \text{Å}} \cdot \left[\frac{0.1\ \mu\text{m}}{L_{\text{eff}}} \cdot \frac{t_{\text{ox}}}{40\ \text{Å}}\right]^3. \tag{2}$$

This implies, for example, that in a structure of 0.1-μm channel length, 40-Å gate oxide, 500-Å junction depth, and 1.0-V power supply voltage, the channel doping has to be $\geq 10^{18}$ cm^{-3}.

The effects of the channel doping on the subthreshold behavior of 0.1-μm devices is illustrated in Fig. 2. For the specified device structure ($t_{\text{ox}} = 40$ Å, $t_j = 550$ Å, $L_{\text{eff}} = 0.1$ μm, and $V_{DD} = 1.5$ V), an N_A of 10^{17} cm^{-3} is not sufficient to suppress short-channel effects, and 10^{18} cm^{-3} dopants are necessary. However, high doping leads to high capacitance in Region (I) of Fig. 1, severely limiting the circuit speed. The surface mobility (in Region (II) of Fig. 1) would also be degraded due to the large vertical fields induced by high doping [5], [8]. Both prob-

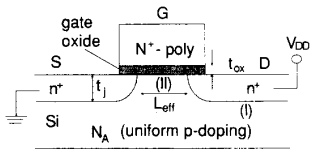

Fig. 1. The device structure for a conventional NMOSFET. A uniform doping of N_A is assumed. Region (I) indicates the junction region, Region (II) the inversion layer.

TABLE I
LIST OF SYMBOLS

L_{eff}	effective channel length
N_A	channel doping
t_{box}	buried oxide thickness
t_j	junction depth
t_{ox}	gate oxide thickness
t_{Si}	silicon-film thickness
V_{bi}	built-in voltage between n^+ source (drain) and the channel
V_{DD}	power supply voltage
V_{ds}	drain-to-source bias
V_{th}	threshold voltage
w_d	drain depletion width
w_s	source depletion width
ϵ_{ox}	dielectric constant of SiO_2
ϵ_{Si}	dielectric constant of Si
$\Phi(x, y)$	potential distribution in silicon film
$\Phi_b(x)$	potential along the bottom interfaces of Si film
$\Phi_f(x)$	potential along the front interface of Si film
Φ_{bx}	$= V_{sub} - V_{FT,b}$, the substrate bias minus the flat-band voltage of the bottom gate
Φ_{gs}	$= V_{gs} - V_{FV,f}$, the gate bias minus the flat-band voltage of the front gate
Φ_{sb}	$= V_{sub}$, the substrate bias (potential)
λ	natural length scale, as discussed in the text

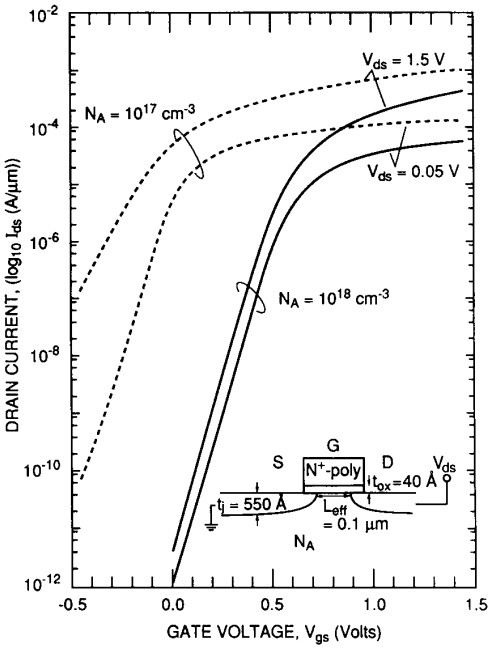

Fig. 2. The effect of the channel doping on the subthreshold behaviors of 0.1-μm devices, as simulated by PADRE. In the inset, $L_{\text{eff}} = 0.1$ μm, $t_{ox} = 40$ Å, $t_j = 550$ Å, and $V_{DD} = 1.5$ V. The channel doping is 10^{17} cm^{-3} (dashed lines) and 10^{18} cm^{-3} (solid lines), respectively. The two curves for each doping are for $V_{ds} = 0.05$ and 1.5 V, respectively.

lems caused by direct scaling—high capacitance and surface mobility degradation—must be solved for deep-submicrometer devices to work successfully.

III. Scaling in Silicon on Insulator

To resolve the problem of high capacitance by direct scaling, the heavy doping has to be reduced in Region (I) of Fig. 1, while maintaining good subthreshold characteristics. One approach is to operate the device at low temperature. The effective barrier height for electrons increases as the temperature decreases [7]. A doping on the order of 10^{17} cm^{-3} can be used at 77 K with good turn-off behavior [9].

Another approach is to use fully depleted SOI [10], as shown in Fig. 3(a). Region (I) in Fig. 1 has now been replaced by a thick buried oxide to reduce the junction capacitance dramatically. Furthermore, the high channel doping can be reduced because of the additional advantage introduced by using a thin Si layer in the structure. Basically, the electrical field profile undergoes a rapid change in the vertical (y-) direction, and induces a large potential curvature in the lateral direction (Fig. 3(c)) helping to build up the potential barrier (Fig. 3(b)) needed to prevent electrons flow from the source [11]. Therefore, one could control horizontal leakage through vertical structures. In the following, we will try to understand such

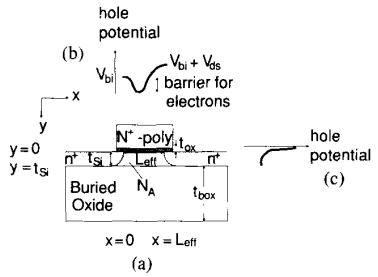

Fig. 3. A fully-depleted SOI MOSFET in the subthreshold regime of operation. (a) Cross-section view of the structure. (b) Lateral potential distribution from source to drain. (c) Vertical potential distribution from the front gate oxide to the bottom buried oxide.

a phenomenon quantitatively, and also look for the possibility of incorporating such a scheme in bulk devices.

Subthreshold conduction is governed by the potential distribution (Fig. 3(b)), which has been studied extensively [3], [12]. We will use the analytic model established by Young [3] in the following discussion. Part of the same analysis will be repeated here for convenience. The potential distribution in the Si film $\Phi(x, y)$ is governed by Poisson's equation

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \tag{3}$$

where $0 \le x \le L_{eff}$ and $0 \le y \le t_{Si}$. The definition of Φ (the hole potential) is such that $\Phi = 0$ coincides with the Fermi level in the most heavily p-doped region. The conduction band is more positive than the valence band. As illustrated in Fig. 3(b) and (c), a smaller Φ corresponds to a larger barrier for electrons. To solve (3), one needs to know the boundary conditions.

The essence of the analytic approach is to simplify the 2D Poisson's equation describing the potential distribution to a one-dimensional (1D) problem of the potential distribution along the top Si/gate oxide interface only. The key elements in the simplification process are the boundary conditions at the bottom Si/buried oxide interface. Different structures have different boundary conditions, and therefore different effects on the potential distributions. Low horizontal leakage requires a large potential difference between the channel and the source, that is a large potential curvature in the *horizontal* direction. High doping levels, for example, would induce a large curvature horizontally as indicated by the right-hand side of (3). One could also try to increase the curvature by making $-d^2\Phi/dy^2$ as large as possible, i.e., to have an abrupt vertical electric field profile (vertical potential curvature). The abruptness in the vertical electric field profile depends on the structure. The following analysis establishes a quantitative relation between the vertical potential curvature and the structure. We first study the conventional SOI structure, Fig. 3(a).

Young [3] used a simple parabolic function in the vertical direction to describe the potential distribution

$$\Phi(x, y) \approx c_0(x) + c_1(x)y + c_2(x)y^2. \tag{4}$$

Such a parabolic function requires three conditions in the vertical direction to have a nontrivial solution, while there appears to be four conditions: the potentials $\Phi_f(x)$ and $\Phi_b(x)$ and fields at $y = 0$ and $y = t_{Si}$. However, since the potential at the bottom interface of the Si film in Fig. 3(a) essentially floats, we relax this condition to simplify the analysis: Furthermore, we assume that the buried oxide thickness is so large that any finite difference induced across it leads to a negligible field. We now have three boundary conditions

1) $\Phi(x, 0) = \Phi_f(x) = c_0(x)$.
2) The electric field at $y = 0$ is determined by the gate voltage and the oxide thickness

$$\left.\frac{d\Phi(x, y)}{dy}\right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} = c_1(x). \tag{5}$$

3) The electric field at $y = t_{Si}$ is approximately zero

$$\left.\frac{d\Phi(x, y)}{dy}\right|_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_{bs} - \Phi_b(x)}{t_{box}}$$
$$= c_1(x) + 2t_{Si}c_2(x) \approx 0. \tag{6}$$

Using these three boundary conditions, we transform $\Phi(x, y)$ to the following expression in which the function $\Phi_f(x)$ is to be solved:

$$\Phi(x, y) = \Phi_f(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y$$
$$- \frac{1}{2t_{Si}} \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y^2. \tag{7}$$

A simpler equation is obtained by substituting (7) into (3), and setting $y = 0$

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{Si}t_{ox}} = \frac{qN_A}{\epsilon_{Si}}. \tag{8}$$

Once $\Phi_f(x)$ is determined, the whole $\phi(x, y)$ can be obtained by using (4). Now we make the following transformation:

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si}t_{ox}} \tag{9}$$

and

$$\phi(x) = \Phi_f(x) - \Phi_{gs} + \frac{qN_A}{\epsilon_{Si}} \lambda^2 \tag{10}$$

which further simplifies (8)

$$\frac{d^2\phi(x)}{dx^2} - \frac{\phi(x)}{\lambda^2} = 0. \tag{11}$$

This is the key equation in our discussion. A natural length scale λ is introduced to describe the potential distribution $\phi(x)$ of the whole structure. Note that $\phi(x)$ differs from $\Phi_f(x)$ only by a position-independent term. Since punchthrough control depends on the potential difference

between the minimum potential in the channel and that of the source, this position-independent term does not affect this difference directly through the potential distribution, but rather indirectly through the boundary conditions as discussed below. And its effect is not as strong as λ.

Equation (11) is simply a second-order 1D differential equation, and can be uniquely solved by specifying two boundary conditions which in our case are the potentials at the source ($x = 0$) and the drain ($x = L_{\text{eff}}$)

$$\phi(0) = V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_{\text{Si}}}\lambda^2 = \phi_s \tag{12}$$

$$\phi(L_{\text{eff}}) = V_{ds} + V_{bi} - \Phi_{gs} + \frac{qN_A}{\epsilon_{\text{Si}}}\lambda^2 = \phi_d. \tag{13}$$

Solving (11) using (12) and (13), we have

$$\phi(x) = \frac{\phi_s[e^{(L_{\text{eff}}-x)/\lambda} - e^{(x-L_{\text{eff}})/\lambda}] + \phi_d[e^{x/\lambda} - e^{-x/\lambda}]}{e^{L_{\text{eff}}/\lambda} - e^{-L_{\text{eff}}/\lambda}}. \tag{14}$$

Note that the approximations used so far are the vertical parabolic function (4) and the zero field at the bottom interface (6). To study the punchthrough behavior, we need information about the minimum potential in the channel, which can be obtained from (14). The minimum will occur at $x = x_{\min}$ by setting

$$\left.\frac{d\phi}{dx}\right|_{x=x_{\min}} = 0$$

$$\phi_s[e^{(L_{\text{eff}}-x_{\min})/\lambda} + e^{(x_{\min}-L_{\text{eff}})/\lambda}] = \phi_d[e^{x_{\min}/\lambda} + e^{-x_{\min}/\lambda}]. \tag{15}$$

Now we assume that the effective channel length is much larger than the natural length scale λ, i.e., $\exp(L_{\text{eff}}/\lambda) \gg 1$. The minimum potential $\phi_{\min}$ then occurs at $x_{\min}$ where

$$x_{\min} \approx \frac{1}{2}L_{\text{eff}} + \frac{\lambda}{2}\ln\left(\frac{\phi_s}{\phi_d}\right) \tag{16}$$

and

$$\phi_{\min} \approx 2\sqrt{\phi_s\phi_d}\, e^{-L_{\text{eff}}/2\lambda}. \tag{17}$$

Note that $\phi(x) = 0$ (10) is the long-channel solution, in which the inversion layer potential is position-independent

$$\Phi_f = \Phi_{gs} - \frac{qN_A}{\epsilon_{\text{Si}}}\lambda^2 \tag{18}$$

as given by Young [13]. Although most of our derivations so far resembles those of [3], [13], the doping-dependent terms have been grouped into the potential representation given by (10). Since the long-channel solution is $\phi = 0$, to obtain a device free of short-channel effects, the potential minimum $\phi_{\min}$ should be as close to zero as possible. Clearly, one way to achieve this is to have a large ratio between L_{eff} and λ, i.e., to operate in the long-channel regime.

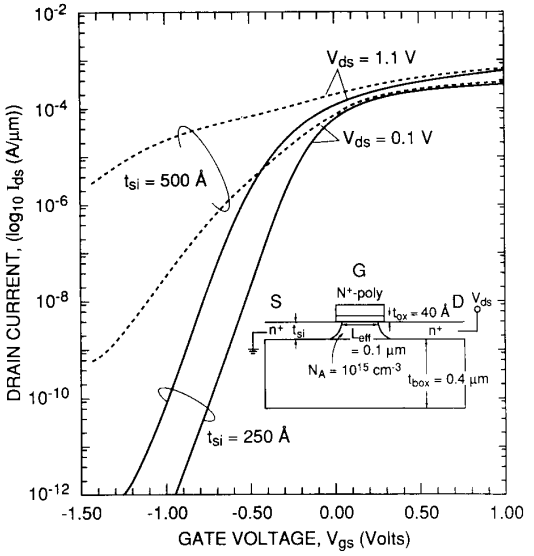

Fig. 4. Subthreshold characteristics of SOI. The device parameters of $L_{\text{eff}} = 0.1$ μm, $t_{ox} = 40$ Å, $N_A = 10^{15}$ cm^{-3}, and $t_{box} = 4000$ Å. The Si film thickness is $t_{Si} = 500$ Å (dashed lines) and 250 Å (solid lines), respectively. The drain-to-source bias conditions are 0.1 and 1.1 V.

Fig. 4 shows subthreshold characteristics calculated by PADRE [4] for SOI devices with $\lambda = 175$ and 250 Å for $t_{Si} = 250$ and 500 Å, respectively. The effective channel length is 0.1 μm. The improvement of the turn-off characteristics by decreasing λ is evident. Although the requirements on the ratio between L_{eff} and λ would depend on the specific application, $\gamma = L_{\text{eff}}/\lambda \approx 5$–10 is generally enough to produce reasonable subthreshold behavior.

We have so far discussed the scaling rule for conventional fully depleted SOI MOSFET's. A natural length scale λ has been introduced (9) as a scaling parameter. To obtain good subthreshold characteristics, the gate length must be longer than λ by a factor determined by the specific application. The role of doping N_A can be understood by studying (12), (13), and (17). For a given λ, an increase of doping (within the range of full depletion) decrease ϕ_s and ϕ_d, helping to reduce $\phi_{\min}$. However, the effect is more or less linear, and it would be more efficient to decrease λ directly. So thin Si films and thin gate oxides are desirable for SOI devices in the deep-submicrometer regime, while the doping would be mainly used to adjust the threshold voltage (10). In the following sections, we will show that λ can be directly controlled through appropriate device design.

The threshold voltage in the long-channel regime is given by $\phi = 0$ and $\Phi_f = V_{bi}$ [13]. From (10), we have

$$\Phi_{gs} = \frac{qN_A}{\epsilon_{\text{Si}}}\lambda^2 + \Phi_f \tag{19}$$

or

$$V_{\text{th}} \approx \frac{qN_A}{\epsilon_{\text{Si}}}\lambda^2 = \frac{qN_A t_{\text{Si}} t_{\text{ox}}}{\epsilon_{\text{ox}}} \tag{20}$$

where we have assumed $V_{FB,f} \approx -V_{bi}$. In the short-channel regime, ϕ is not zero, but positive. And the threshold voltage is smaller by ϕ, as can be seen from (10). Note that (20) reproduces the threshold voltage expression given in [13].

IV. Other SOI Structures: Gate-All-Around

In the previous section, the boundary conditions play an important role in determining the natural length scale λ. If, for example, we change the structure from Fig. 3 (Fig. 5(a)) to Fig. 5(b) or Fig. 5(c), the boundary conditions will change, and therefore λ, if present, would also change.

The *Gate-All-Around* structure (Fig. 5(b)) has been proposed as a way to improve the drive capability of SOI devices [14], [15]. Basically, the buried oxide is replaced by a gate oxide, and the same gate voltage is applied to both the top and bottom gates. Following the same analysis as in the last section, we again simplify the 2D Poisson's equation into a 1D problem. Due to the change of the boundary condition at the bottom interface, a different equation is obtained. The natural length scale λ is reduced through such a structure change. The boundary conditions of 1)–3) for Fig. 5(b) are as follows:

1′) $\Phi(x, 0) = \Phi(x, t_{Si}) = \Phi_f(x) = \Phi_b(x) = c_0(x)$.
2′) The electric field at $y = 0$ remains the same as 2).
3′) The electric field at $y = t_{Si}$ is the same as that at $y = 0$ but opposite in sign

$$\left.\frac{d\Phi(x, y)}{dy}\right|_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_{gs} - \Phi_f(x)}{t_{box}} = c_1(x) + 2t_{Si}c_2(x) = -c_1(x) \quad (6')$$

where the most important change is that we now have $c_2(x) = -c_1(x)/t_{Si}$, instead of $c_2(x) = -c_1(x)/2t_{Si}$ as in (6). Equation (7) now becomes

$$\Phi(x, y) = \Phi_f(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y - \frac{1}{t_{Si}} \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f - \Phi_{gs}}{t_{ox}} y^2 \quad (7')$$

and the key difference between (7) and (7′) is the factor of 2 in the third term of (7) is removed in (7′). This effectively reduces the Si film thickness by a factor of two, and the natural length scale becomes

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} t_{Si}t_{ox}}. \quad (9')$$

This means that, for the same effective channel length this structure would have better subthreshold behavior than the structure of Fig. 3 (or Fig. 5(a)). The minimum channel length for good subthreshold characteristics can thus be made about 30% shorter by going from the conventional SOI structure to Gate-All-Around.

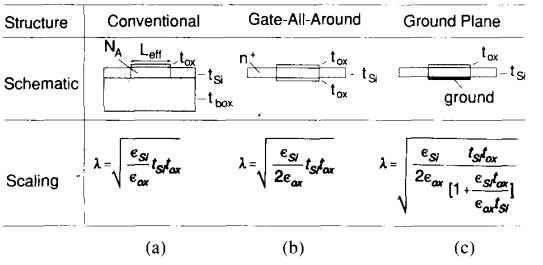

Fig. 5. Various SOI structures: (a) Conventional, (b) Gate-All-Around, and (c) Ground-Plane. The structures are schematically shown in the second row, the natural length scales in the third row.

The threshold voltage is similarly given by (20), except that λ in (9′) should be used. In other words, we have

$$V_{th} \approx \frac{qN_A}{\epsilon_{Si}} \lambda^2 = \frac{qN_A t_{Si} t_{ox}}{2\epsilon_{ox}}. \quad (20')$$

This result agrees with [14].

V. Pulse-Shaped Doping

We showed in the previous section that the scaling rules for SOI devices can be modified by changing the device structure. The structure of Fig. 5(b) behaves better than that of Fig. 5(a) in terms of scaling the gate length. The Gate-All-Around structure introduces additional symmetry in the structure, with a zero field occuring in the middle of the Si film, halfway between the top and bottom gates. Therefore, the effective Si film thickness is reduced to half the actual thickness. A similar effect can be obtained by fixing the bottom interface at a fixed potential, e.g., ground, as shown in Fig. 5(c): the *Ground-Plane* structure. The boundary conditions are as follows:

1″) The surface potential remains the same as 1).
2″) The electric field at $y = 0$ remains the same as 2).
3″) The potential (not the electrical field) at $y = t_{Si}$ is Φ_{sb}

$$\Phi(x, y)|_{y=t_{Si}} = \Phi_{sb} = c_0(x) + t_{Si}c_1(x) + t_{Si}^2 c_2(x) \quad (6'')$$

and (7) becomes

$$\Phi(x, y) = \phi_f(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y - \frac{1}{t_{Si}} \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} \cdot y^2 - \frac{\Phi_f(x) - \Phi_{sb}}{t_{Si}^2} y^2. \quad (7'')$$

Note that in addition to the removal of the factor of 2 in the third term of (7), there is one more term (the fourth term) that decreases λ further. This reduction can be observed more clearly by rewriting (8) as

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{2(\Phi_f(x) - \Phi_{gs})}{t_{Si}t_{ox}} - \frac{2(\Phi_f(x) - \Phi_{sb})}{t_{Si}^2} = \frac{qN_A}{\epsilon_{Si}}. \quad (8'')$$

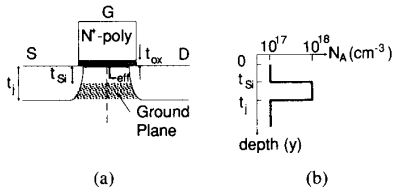

Fig. 6. The Pulse-Shaped Doped structure. (a) Cross-section view of the structure. (b) Vertical doping profile. The example used in Fig. 7 has L_{eff} = 0.1 μm, t_{ox} = 40 Å, t_{Si} = 250 Å, t_j = 500 Å, and the doping profile shown in Fig. 6(b).

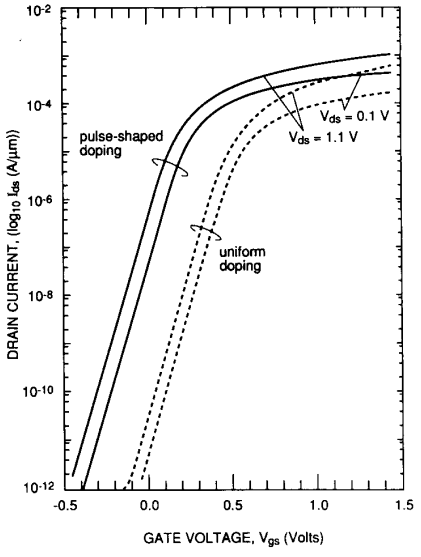

Fig. 7. Subthreshold characteristics of PSD (solid lines) shown in Fig. 6, and the uniform doping structure (dashed lines) with $N_A = 10^{18}$ cm^{-3} shown in Fig. 1. The drain-to-source bias conditions are 0.1 and 1.1 V.

And the same (11) can again be obtained by the following transformation:

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} \frac{t_{Si} t_{ox}}{1 + (\epsilon_{Si} t_{ox} / \epsilon_{ox} t_{Si})}} \qquad (9'')$$

and

$$\phi(x) = \Phi_f(x) + \frac{qN_A}{\epsilon_{Si}} \lambda^2 - \left(\frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{2}{t_{Si} t_{ox}} \Phi_{gs} + \frac{2}{t_{Si}^2} \Phi_{sb} \right) \lambda^2. \qquad (10'')$$

The extra term in (9″) is interesting. For a 40-Å gate oxide and a 250-Å Si film, λ decreases from 175 to 124, to 101 Å when the structure changes from Fig. 5(a) to Fig. 5(b), to Fig. 5(c). Therefore, the Ground-Plane structure (Fig. 5(c)) gives a 75% improvement in λ over the conventional fully depleted SOI and a 20% improvement in λ over the Gate-All-Around structure.

The threshold voltage in the long-channel regime occurs when $\phi = 0$ and $\Phi_f \simeq V_{bi}$. From (9″, 10″)

$$V_{th} \approx \frac{qN_A t_{Si} t_{ox}}{2\epsilon_{Si}} + \frac{\epsilon_{Si}}{\epsilon_{ox}} \frac{t_{ox}}{t_{Si}} V_{bi}. \qquad (20'')$$

The second term is due to the ground-plane configuration.

One important aspect of the Ground-Plane structure is that it can be realized in bulk Si. Fig. 6(a) shows the bulk implementation of Fig. 5(c), and Fig. 6(b) shows one example of the doping profile for such an implementation. Because the doping profile resembles a pulse from the surface to the substrate, we name the structure *Pulse-Shaped Doped*, or PSD. Fig. 7 is a PADRE simulation for the PSD structure shown in Fig. 6. The simulation for a structure with a uniform doping of 10^{18} cm^{-3} is also shown in Fig. 7 for comparison. The subthreshold behavior of the uniform-doping structure is preserved in PSD. The threshold voltage of PSD is lower because some dopants are removed from Region (II) of Fig. 1. Note that the doping in Region (I) of Fig. 1 is reduced by a factor of ~10, and the capacitance is reduced by a factor of more than 3. Other simulations indicate that the threshold voltage can be adjusted by adjusting the doping level in the channel (Region (II)) without changing the subthreshold behavior, as predicted in (20″).

VI. Fabrication of PSD Structures

PSD resembles retrograde [16] and punchthrough control implants [17], controlling the horizontal leakage through vertical doping profiles. The concept here is to reduce the doping from that of a uniformly doped structure (Fig. 1). And the guideline is not to implant dopants into the channel region arbitrarily, but to mimic a modified, fully depleted SOI structure: the Ground-Plane structure. Since we have derived the scaling rule from the conventional SOI structure, the placement of the heavily doped region is part of the scaling. Another similar structure is the low-impurity-channel transistor (LICT) [18]. The difference here is that PSD has a light doping below the junctions, in addition to the lightly doped channel. The threshold voltage for both PSD and LICT depends on the position of the heavy implant region (see (20″)), as well as on the doping level itself. As long as the junction is not deeper than the heavily doped region, the scaling rule would depend only on the lightly doped Si layer (film) thickness. This relaxes the requirements on the junction depth to some extent, provided the heavily doped region can be maintained down to the junction depth. Thus we have shown that conventional scaling rules in bulk Si can be substantially modified to advantage through the introduction of new, but realistic designs. The guidelines for these designs are based on the theoretical framework described above.

Since the PSD structure has a highly doped region sandwiched between two lightly doped regions, one can either use a single implant to create a heavily doped re-

gion, or use both n and p dopants to tailor the overall profile. The structure can be epitaxially grown and doped to create the rapidly varying vertical profile. Note that a single implant would work better for PMOSFET's, because the diffusion of As or Sb is much slower than B.

VII. Conclusion

As device dimensions penetrate into the deep-submicrometer regime, conventional MOSFET scaling rules lead to excessively high doping requirements, causing undesirably large junction capacitances and degraded mobility. The junction capacitance difficulty can be alleviated by using fully depleted silicon on insulator devices. By studying the scaling of SOI devices, we have established a single theoretical framework within which both bulk and SOI structures can be understood. This framework yields a natural length scale which can be effectively used as a design guideline. It also provides ways to mimic SOI structures and concepts in bulk Si. As a result, we have proposed the concept of *Pulse-Shaped Doping*, an innovative but realistic device design, that promises well-behaved operation of devices in the deep-submicrometer regime.

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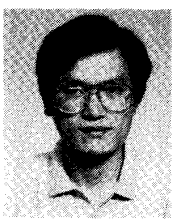

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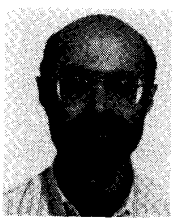

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