

University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #1

Due Date: Feb 22nd, 10 pm, via email to arnab@ucsb.edu

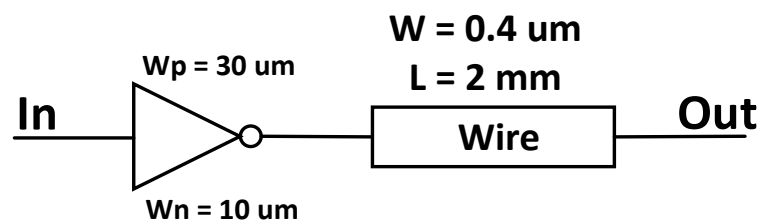
Problem 1 – CMOS Design (20 pts) (2+2+2+2+6+6)

Draw the transistor level schematic of a 4-1 Multiplexer with:

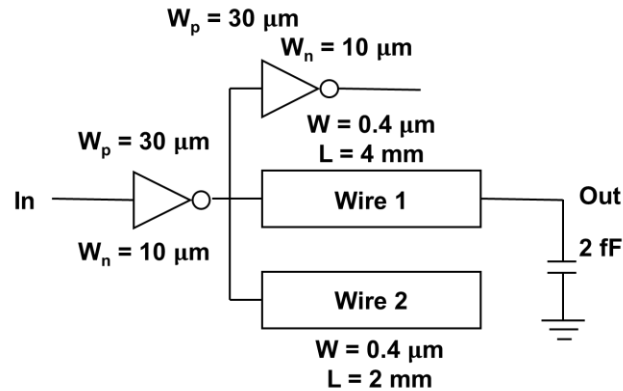
- transmission gate
- pass transistor logic
- pass transistor with restoring logic
- static CMOS
- Implement all above logic families in Hspice, use 65 nm technology. Compare power, delay and power-delay product of different multiplexers in room temperature.
- Change temperature to 100°C and repeat part (e).

Problem 2 – Interconnect and Repeater Insertion (20 pts)

a) The following figure shows an inverter driving a piece of wire. Assume that all transistors are minimum channel length ($L = 0.25 \mu\text{m}$) and have the following characteristics: gate capacitance $C_G = 2 \text{ fF}/\mu\text{m}$, drain capacitance $C_D = 1 \text{ fF}/\mu\text{m}$, and channel resistance $R_{sqn} = R_{sqp}/2 = 15 \text{ k}\Omega/\text{Square}$. For the wires, assume that: parallel plate capacitance $C_{wpp} = 0.1 \text{ fF}/\mu\text{m}^2$, fringing capacitance $C_{wfringe} = 0.05 \text{ fF}/\mu\text{m}$ per edge, and wire resistance $R_w = 0.2 \Omega/\text{Square}$.



- Draw the RC model you would use to calculate the delay of the circuit shown above from **In** rising to **Out** falling. Replace the wire with a single section π model and calculate the values of the resistance and capacitance in your model.
- What is the Elmore delay from **In** rising to **Out** falling?
- What is the Elmore delay of the circuit shown below (from **In** rising to **Out** falling)?
- Evaluate the delay from In to Out for the circuit shown below:



b) Read the paper posted under Lecture 6, “A Power-Optimal Repeater Insertion Methodology for Global Interconnects in Nanometer Designs”, and answer the following questions:

- i. How will you estimate a uniform interconnect buffered by identical repeaters? Replot Fig. 1 with the latest IRDS report (you can download it at: [How to Download IRDS™ Reports - IEEE IRDS™](#)).
- ii. What are the different components of the power dissipation of the inserted inverters in the paper? How will you estimate total power consumption of the inserted inverters?

Problem 3 - MOSFET Physics and Short Channel Effects

Consider a n-type MOSFET with a p-substrate. As we keep reducing the channel length of the transistor, we run into several short channel effects where the control of the gate on the channel potential is reduced, and the drain starts affecting the channel potential. This leads to degradation in the transistor performance metrics and is very critical as technology nodes keep going down. Here we are going to discuss several of the short channel effects in a conventional MOSFET and their solutions.

- a) Explain with the help of the energy band diagrams what is meant by Drain Induced Barrier Lowering (DIBL) and Gate Induced Barrier Lowering (GIDL). How is DIBL different from GIDL? Which structural parameters of transistors make it more susceptible to GIDL compared to DIBL?
- b) How can high-K dielectrics and strain engineering help us overcome the short channel effects? Discuss the straining of the channel material of modern FinFETs.
- c) Sketch the curve of carrier velocity vs. lateral electric field for a device in which velocity saturation occurs and briefly describe the cause of velocity saturation.
- d) What is the main difference between Schottky contact and Ohmic contact? How can you change a Schottky contact to an Ohmic one?

Problem 4 - MOSFET Electrostatics

Read the paper on MOSFET scaling (R. H. Yan et al., “Scaling the Si MOSFET: From Bulk to SOI to Bulk,” IEEE Transactions on Electron Devices, vol. 39, no. 7, pp. 499-502, 1992.). Derive the expressions for the Natural Length (λ) for the following devices:

- a) Planar Bulk MOSFETs (with and without high-k dielectric)
- b) Ultra-thin Body (UTB) SOI MOSFETs (partially depleted and fully depleted)
- c) Double-gate FETs: (FinFET) and Tri-gate FET
- d) Gate-all-around nanosheet transistors (or a nanowire FET)
- e) MOSFETs with 2D-channel materials.

What do you think are the limitations of such analyses based solely on the surface potential?

Problem 5 Power Dissipation in a Circuit

- (a) When we talk about power consumption in a circuit, we talk about its various components – Dynamic power, leakage power, static power, and short circuit power. Explain the difference between each of these power dissipation mechanisms and give solutions (you may take help of equations if necessary) how can we alleviate each of them.
- (b) Derive the minimum voltage swing required for switching a CMOS inverter and pseudo NMOS (Hint: it is few kT/q).
- (c) In each case, how would the answer change if we have a chain of such gates, say 11 in a ring oscillator or other cascaded structures with multiple stages?