University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #2

Due Date: March 8th, 10 pm via mail to arnab@ucsb.edu

Question 1 – Tunneling FETs

Please review lecture 11, slide 11 showing the slow V_{ds} turn-on.

a) Why the I_D-V_D is not linear at low V_D regime? Is this an intrinsic or extrinsic property? Is there any possibility to eliminate it? If tunnel FETs are used to design a 1T-DRAM, what effect could be expected?

b) Analyze the enhanced Miller effect in a tunnel FET based inverter with load capacitance, reproduce the figure (showing Miller effect) by SPICE simulation. (hint: you can use MOSFETs instead of tunnel FETs in the simulation, and artificially change the capacitance).

c) Discuss the effects of channel length scaling in TFETs? How will the minimim and average SS vary with channel length?

d) What are the advantages of 2D semiconductor channel materials for designing TFETs?

Question 2 –Device Variations (20 pts)

a) What is the origin of Work-function Variation (WFV)? What is the state-of-the-art in terms of mitigating or dealing with WFV?
b) Make a table of relevant gate metals from the literature and comment on their WFV as channel length is scaled down.
c) Discuss WFV and any other sources of intrinsic variations in emerging transistors.
d) In the paper titled "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic OR gates" by H. Dadgour, briefly explain what the motivation for the keeper circuit is.
e) Explain how the process variation sensor circuit works.

Question 3 – Non-conventional memory technologies (20 pts)

Summarize (using a Table) the scaling challenges for different types of memories, including **SRAM**, **DRAM**, **flash memory**, **3D-NAND**, **memristor**, **Phase Change Memory (PCM)**, **Spin Torque Transfer Magnetic Memory (STT-MRAM)**, **Resistive Memory (RRAM)**, **Conductive-bridging Memory (CBRAM)** and **Ferroelectric RAM (FeRAM)**. Discuss the advantages and disadvantages of these emerging memory technologies in different applications.

Question 4 – Three-Dimensional Integration (20 pts)

Read the article on 3D integrated circuits, by *Banerjee et al., Proceedings of IEEE, 2001*, and answer the following questions.

1. What are the benefits of 3D integration?

2. Prepare a table summarizing various 3D ICs introduced so far by commercial entities and their timelines. What is the total 3D IC market (in billions of dollars) and what are the projections?

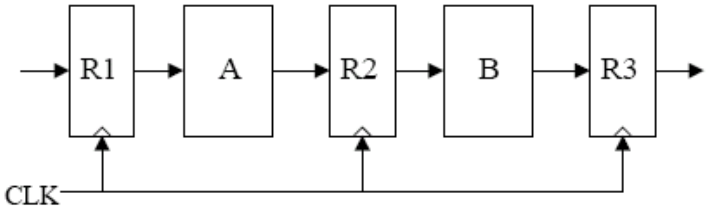
3. What are the current 3D IC fabrication methods? List the various challenges?

4. What are the benefits of monolithic 3D integration? Why are 2D materials beneficial for monolithic 3D integration?

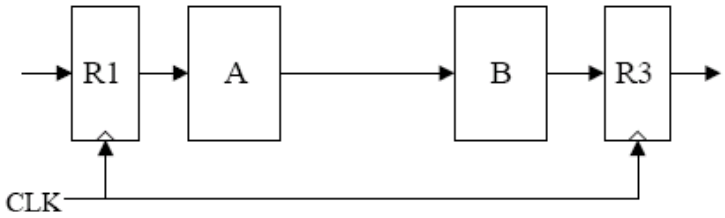
Question 5 – Clock Distribution and Pipeline Timing (20 pts)

The registers have hold time 0 ns, clock-to-Q delay 0.6 ns, and setup time 0.4 ns. The logic delays for logic blocks A and B are given below. Some outputs from A or B may be available as soon as t_{min} or take as long as t_{max}. And the inputs to A or B must be stable for at least t_{max} to guarantee a correct output generated. Unfortunately, t_{max} cannot be reduced for either logic block.

Block A: t_{min} = 2.0 ns, t_{max} = 2.4 ns
Block B: t_{min} = 1.2 ns, t_{max} = 1.4 ns



The middle register can be removed to save a little bit of time. In this case, the registers are clocked faster than the total delay through A and B, and there are two different data flowing through the logic at any time. i.e., on one clock edge datum is launched into A. As that datum flow goes into B, a new datum is launched into A. Two periods after it is launched, the first datum has reached the output of B and is latched, and the second datum is going from A to B.



a) What is the minimum clock period?
b) What is the maximum clock period?
c) If this pipeline operates correctly at 400 MHz, what is the minimum t_{min} for block A?
d) What are the drawbacks/limits of this technique?