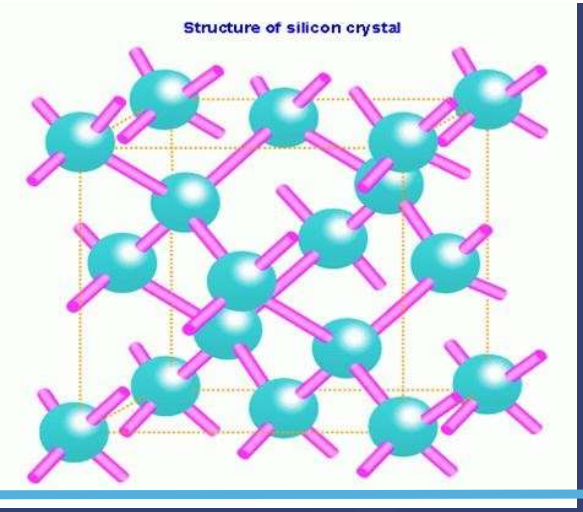
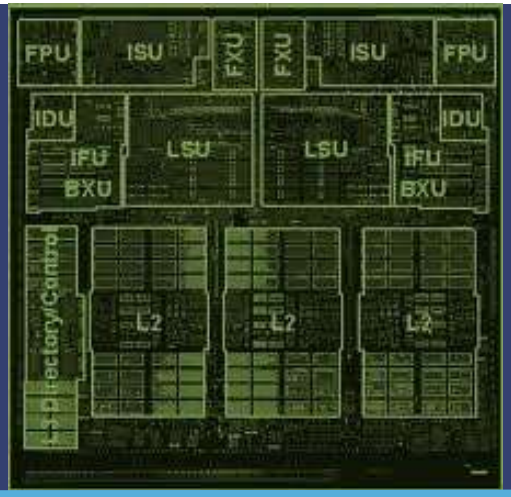
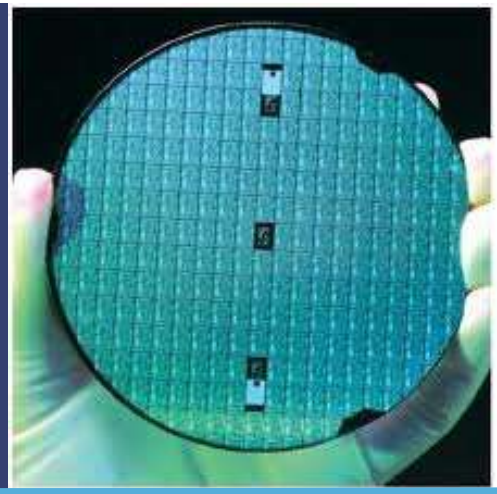


# ECE 225
# Lecture 15
# 3-D Integrated Circuits

*Prof. Kaustav Banerjee*
*Electrical and Computer Engineering*
*University of California, Santa Barbara*

# Outline

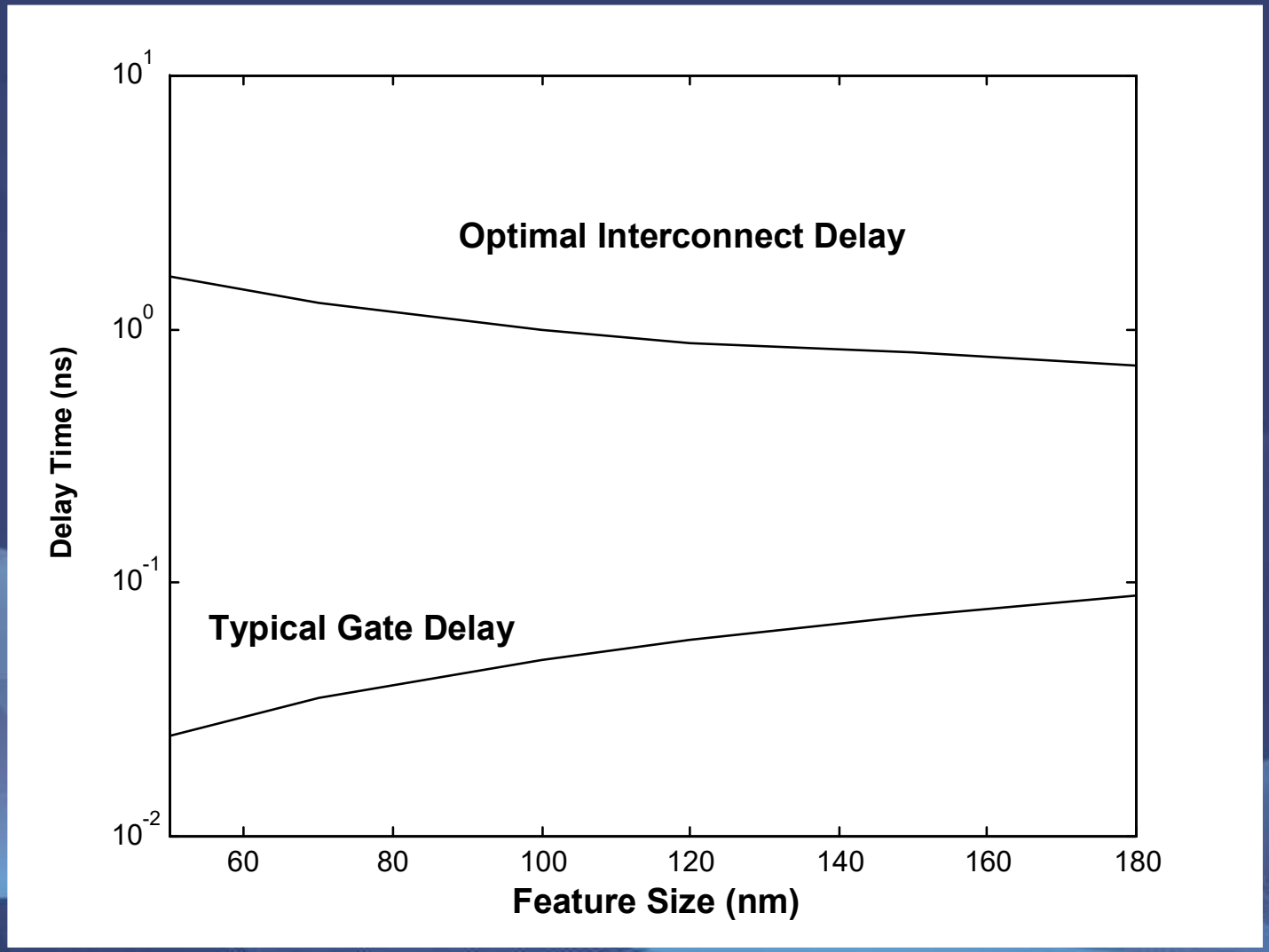
- Motivation for 3-D ICs
- Performance Analysis
- Thermal Analysis
- Technologies for 3-D ICs
- Applications and Innovations
- Summary

# Motivation for 3-D ICs

- Increasing Chip Size and Interconnect Delay
- Limitations of Cu/Low-k
- Limitations of Repeaters
- Effects on Design Process
- Heterogeneous Integration

K. Banerjee et al., Proceedings of the IEEE, Vol. 89, No. 5, May 2001

# Interconnect Delay is Increasing (ITRS '99)



# Will better materials like copper and low-k dielectrics solve the interconnect problem?

# Low-k Dielectrics

## IBM Says Process Can Make Chips More Powerful

*By Bruce Meyerson*
ASSOCIATED PRESS

NEW YORK — IBM Corp. has developed a method for insulating the tiny circuits on a computer chip so they can be placed even closer together, making room for more computing power on each semiconductor.

The new process, which coats the circuits with a chemical polymer instead of silicon dioxide, can either improve a chip's processing speed by as much as 30 percent or halve the amount of power it uses, IBM said yesterday.

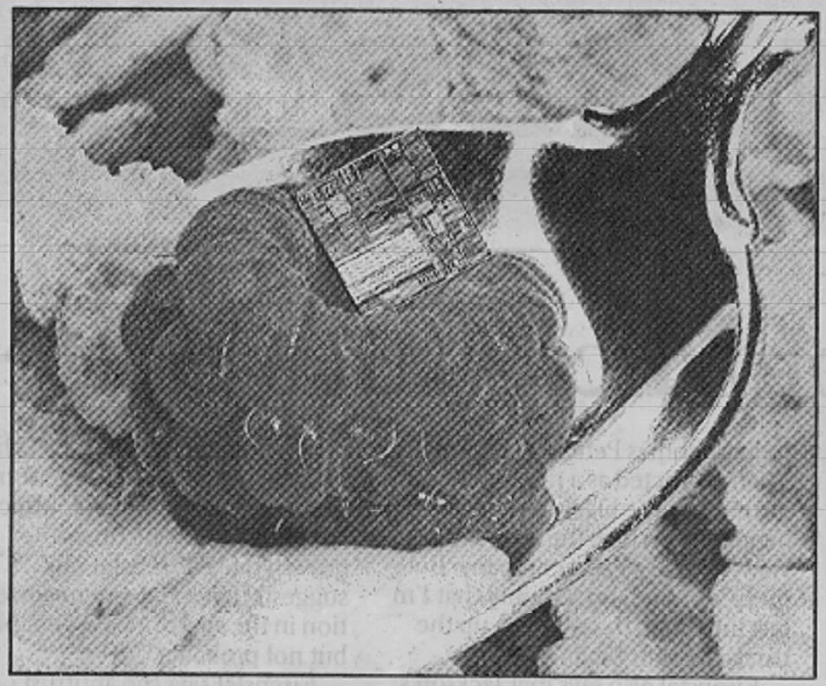
The insulation cuts down on magnetic interference, or "crosstalk," between the electrical pulses that travel along the millions of copper circuits that a chip uses to crunch data.

Because the electrical pulses are better shielded from the magnetic fields generated by neighboring pulses, the distance between circuits can be reduced by more than a quarter to 0.13 microns — a measurement 600 times thinner than a human hair.

Thanks to the space savings, chipmakers can double the number of transistors they cram onto a piece of silicon to about 400 million, said Bijan Davari, a vice president of IBM's semiconductor research and development center in East Fishkill, N.Y.

Chips made with the new insulation are expected to be available next year, IBM said.

The first application will be to produce powerful microprocessors for major business systems like those used to run Web sites and communications networks.



Associated Press

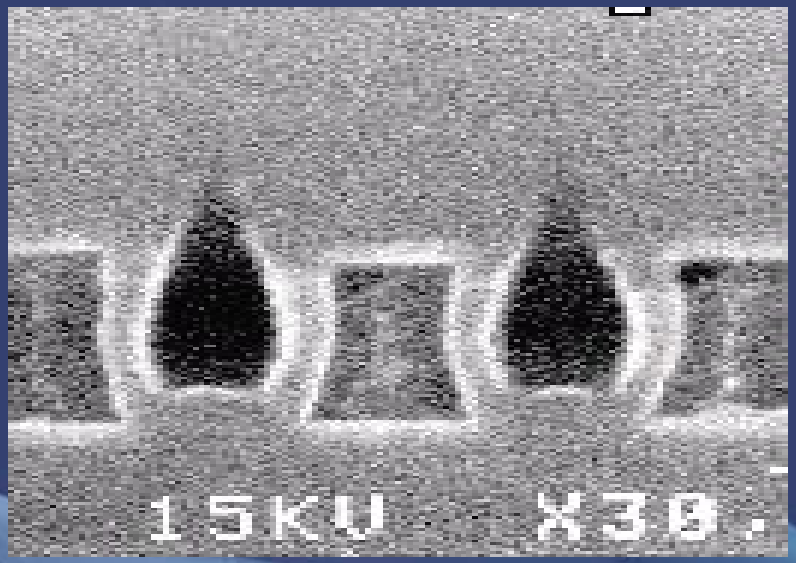
IBM said its new process for insulating circuits on small computer chips (such as this planted in a spoon of fruit and cereal for size comparion) should increase computing speed and performance by as much as 30 percent.

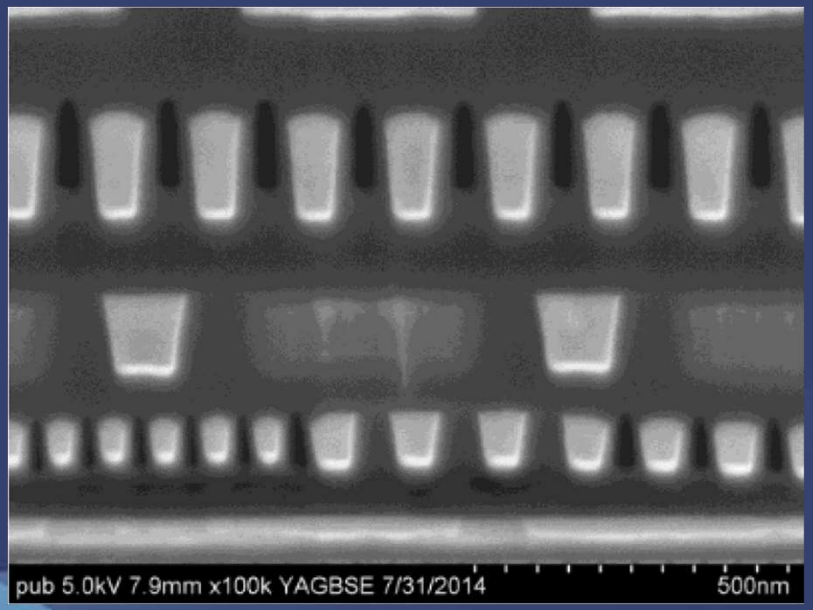
Old dielectric $SiO_2$ K = 4

New dielectric Silk K = 2.5

The difference is not even a factor of 2!

# Limit of Low-k Dielectrics (Air: K =1)



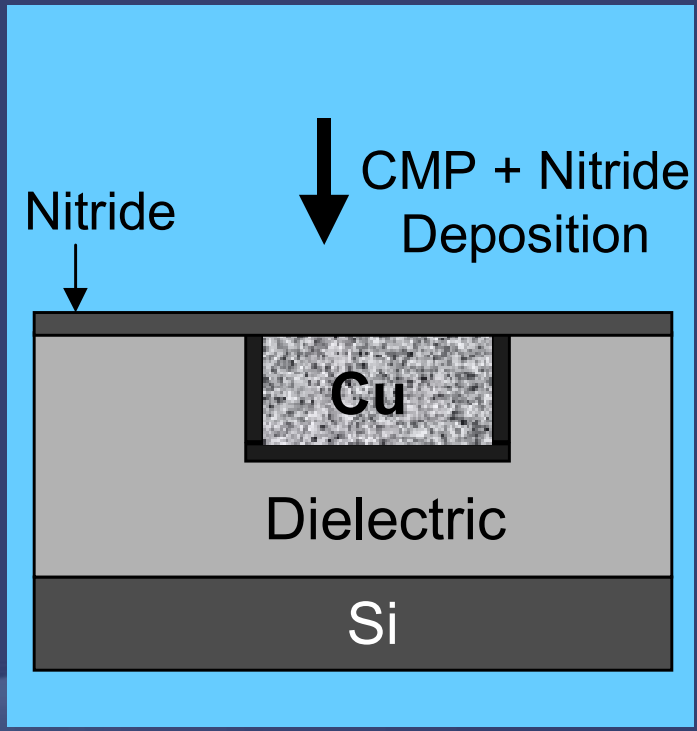




Intel's 14nm Logic Technology
(2014 IEDM)

Air-Gap Interconnect Structure

# Cu Resistivity: Effect of Scaling

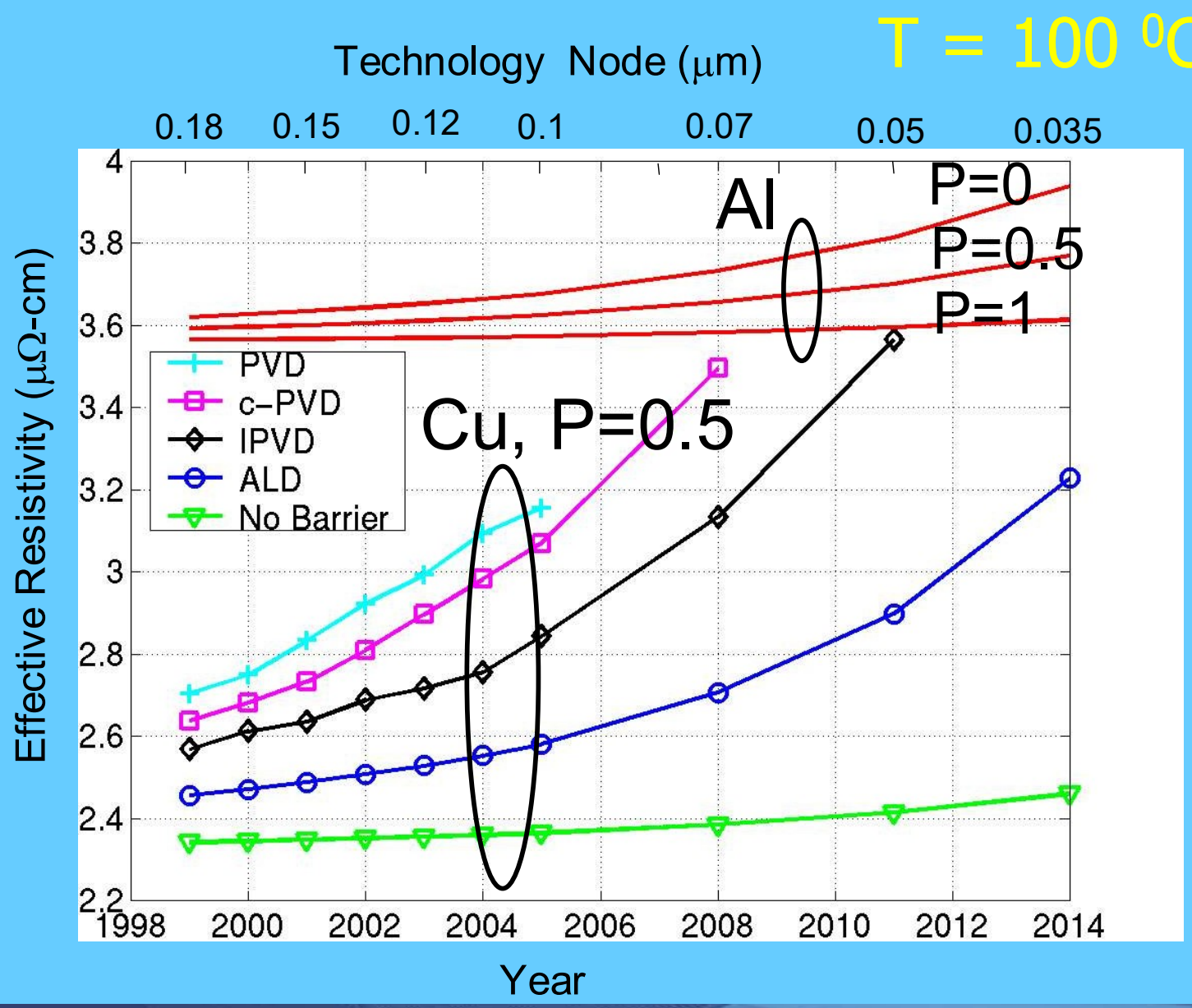
- Effect of Cu diffusion Barrier
  - Barriers have higher resistivity
  - Barriers can't be scaled below a minimum thickness



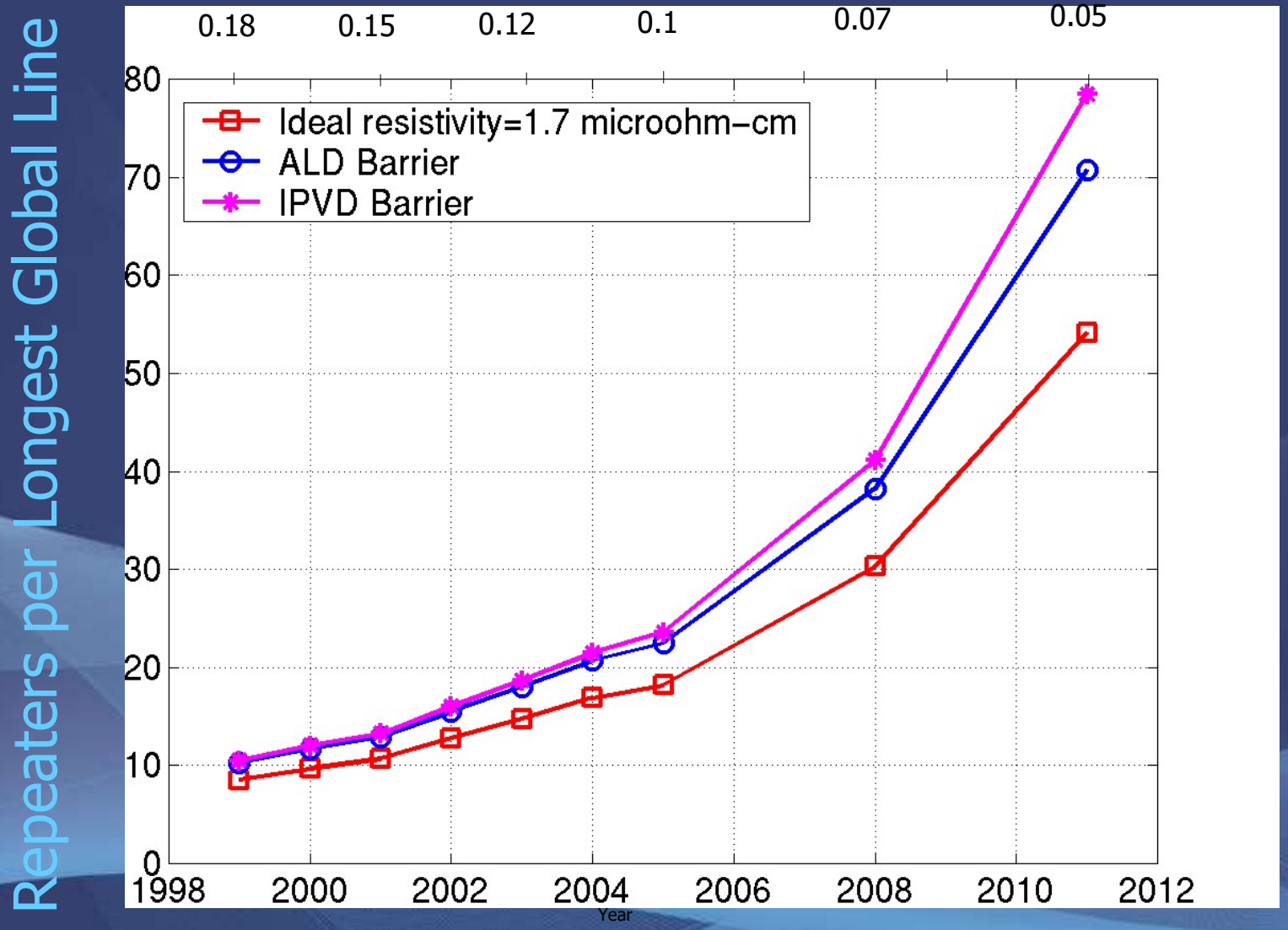

- Effect of Electron Scattering
  - e scattering from the surface
  - increases effective resistivity

Problem is worse than anticipated in the ITRS roadmap

# Cu Resistivity: Effect of Scaling

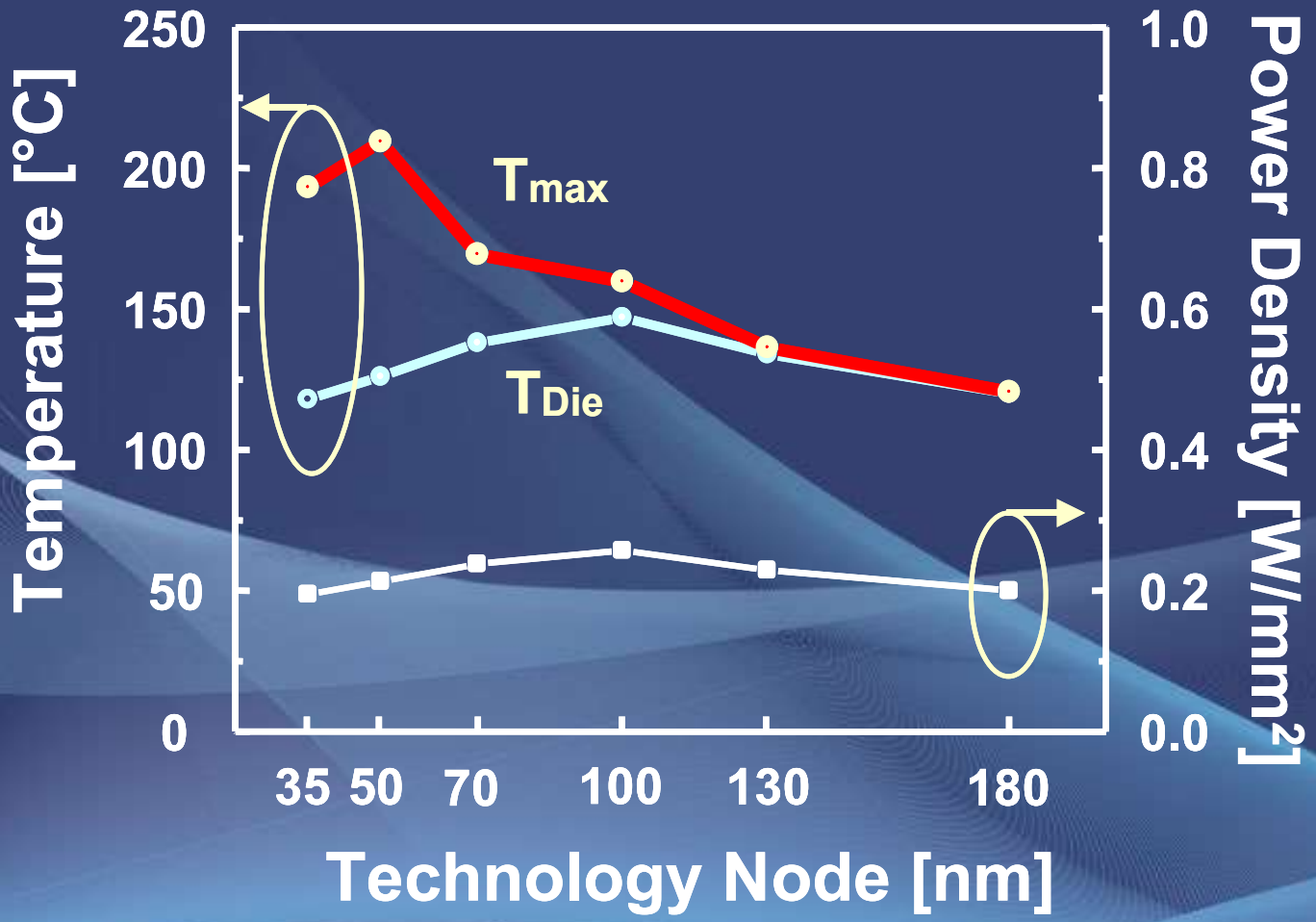


# Cu Resistivity: Effect of Scaling



# Scaling Effects: Maximum Chip Temperature

(S. Im and K. Banerjee, IEDM 2000)

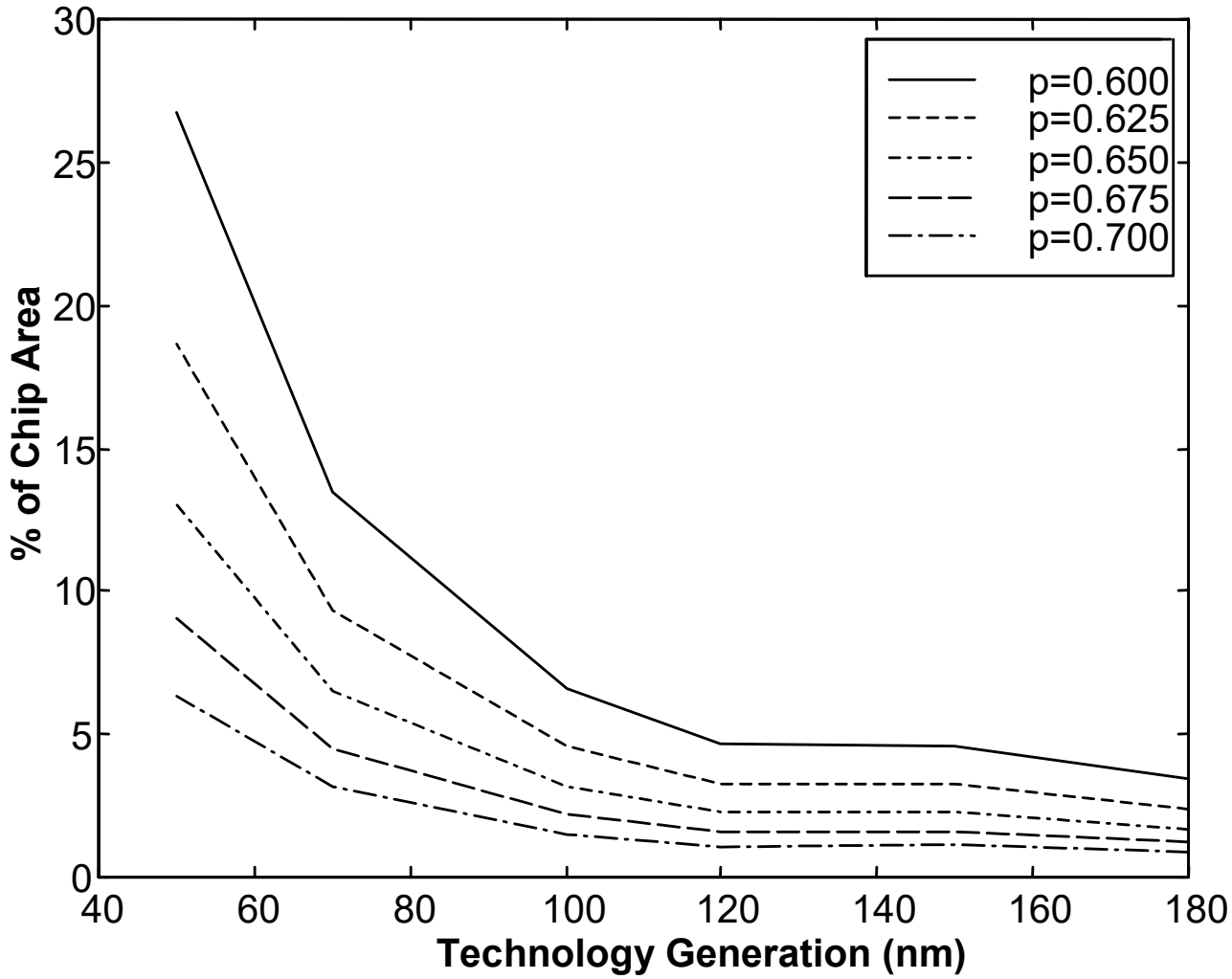



- Negligible Change in Power Density ( ITRS '99 )
- Increase in $T_{max}$ Due to Joule Heating of Interconnects ( FEM Simulation )

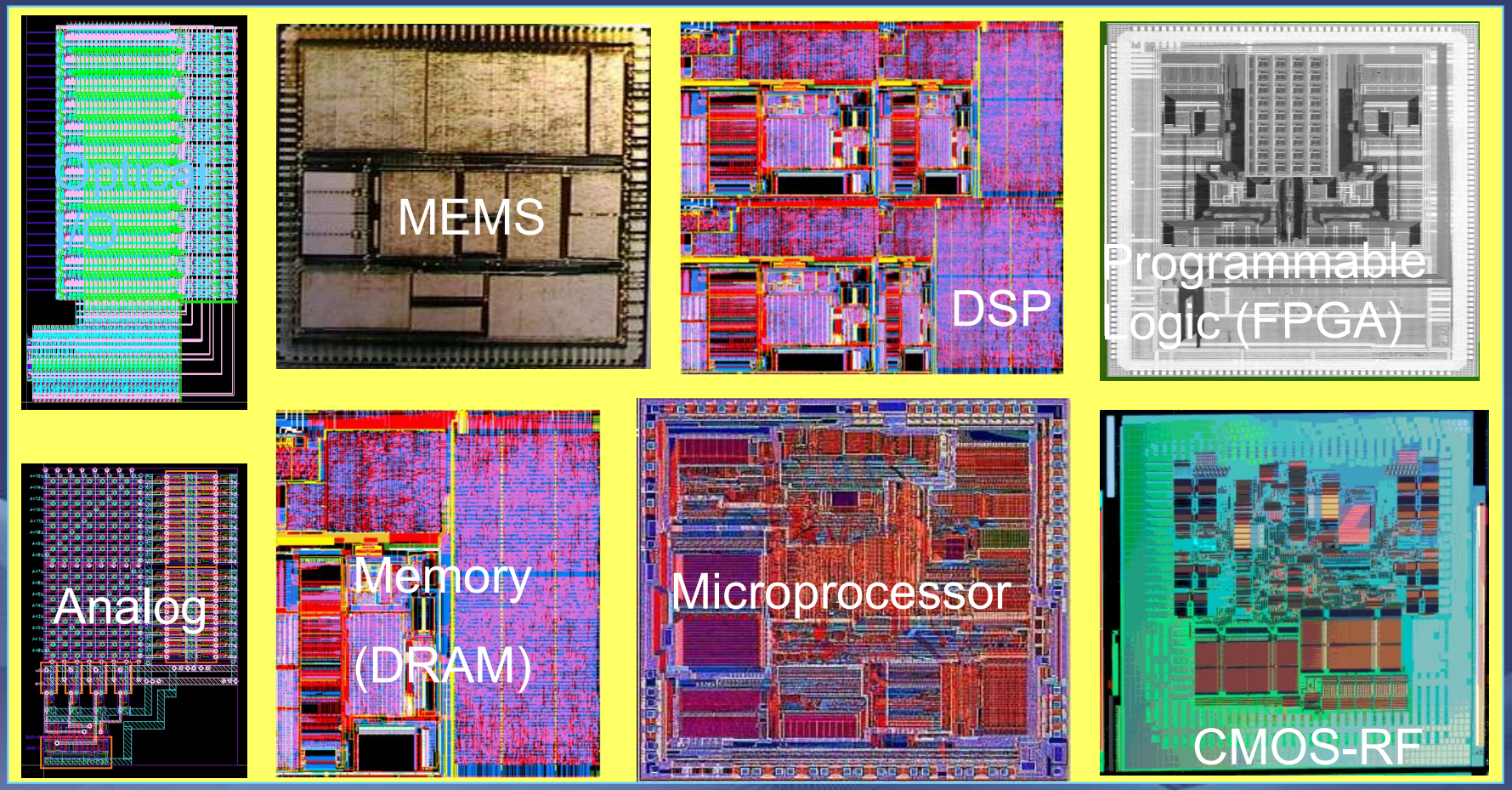
# Effects on Design Process

- Increasing wire delay causes timing closure problem
- Prevents CAD methodologies to adopt higher levels of abstraction to simplify and accelerate the design process

# Can we solve the problem by using more repeaters?

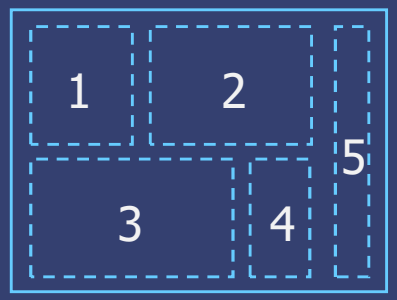


# Integrated SoC to Sense, Process, and Collaborate

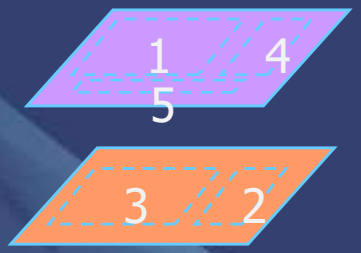



Difficult in Planar IC Technology

# Novel Design Architectures Needed!




Single Layer




2 Layers

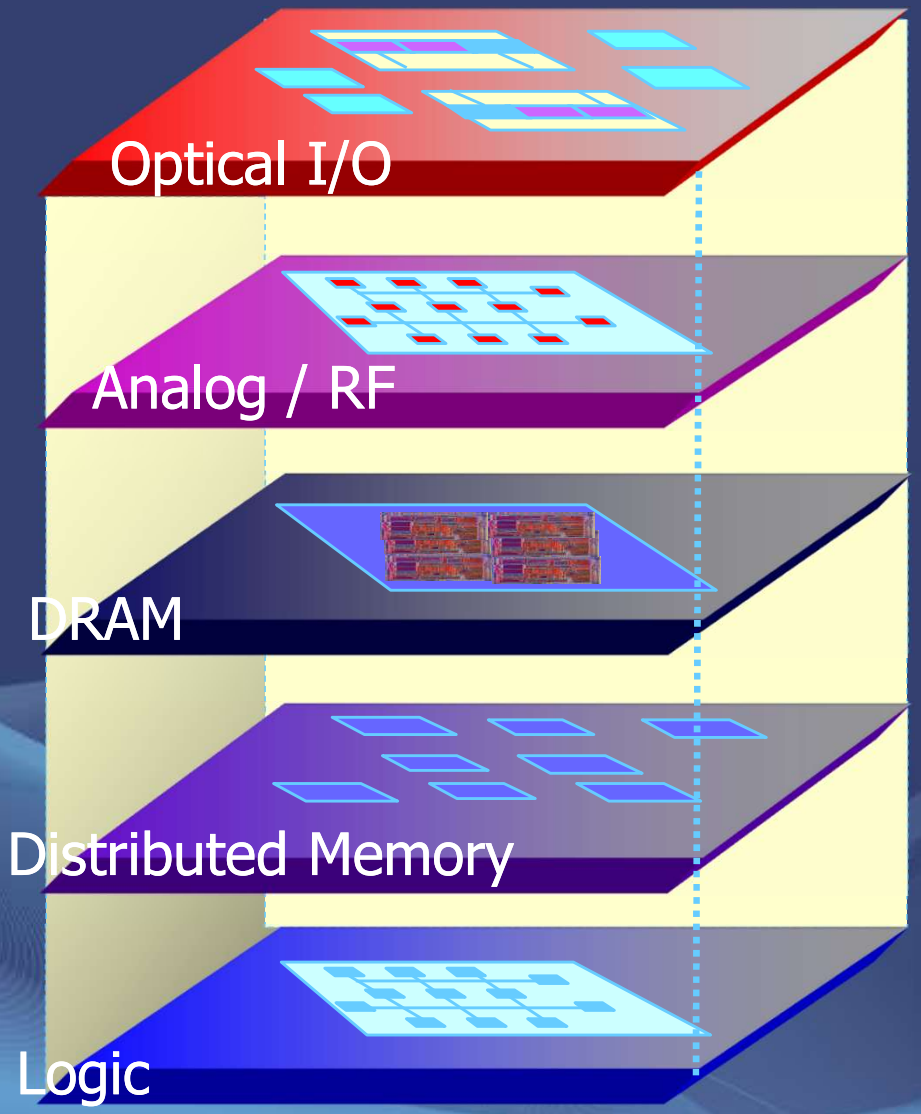
Replace horizontal by vertical interconnect

3-D ICs utilize the vertical dimension

# 3-D ICs : Multiple Active Si Layers

(Banerjee et al., Proc. IEEE, 2001)

- Advantages
  - Reduce Interconnect Length by Vertically Stacking Multiple Si Layers….lower power
  - Improve Chip Performance
  - Reduce Chip Area
  - Heterogeneous integration possible, e.g., memory, digital, analog, optical, etc.



# Performance Analysis Strategy

- Estimate Chip Area
- Estimate Interconnect Delay

Chip Area Determined from Wiring Requirement

Used 50 nm ITRS Data

# Wire-Length Distribution

Calculate # of Interconnects of length l

T represents number of signal input and output (I/O) pins

number of interconnects is proportional to T

- Conservation of I/O's

$$T_A + T_B + T_C = T_{A\text{-to-}B} + T_{A\text{-to-}C} + T_{B\text{-to-}C} + T_{ABC}$$

$$T_A + T_B = T_{A\text{-to-}B} + T_{AB}$$

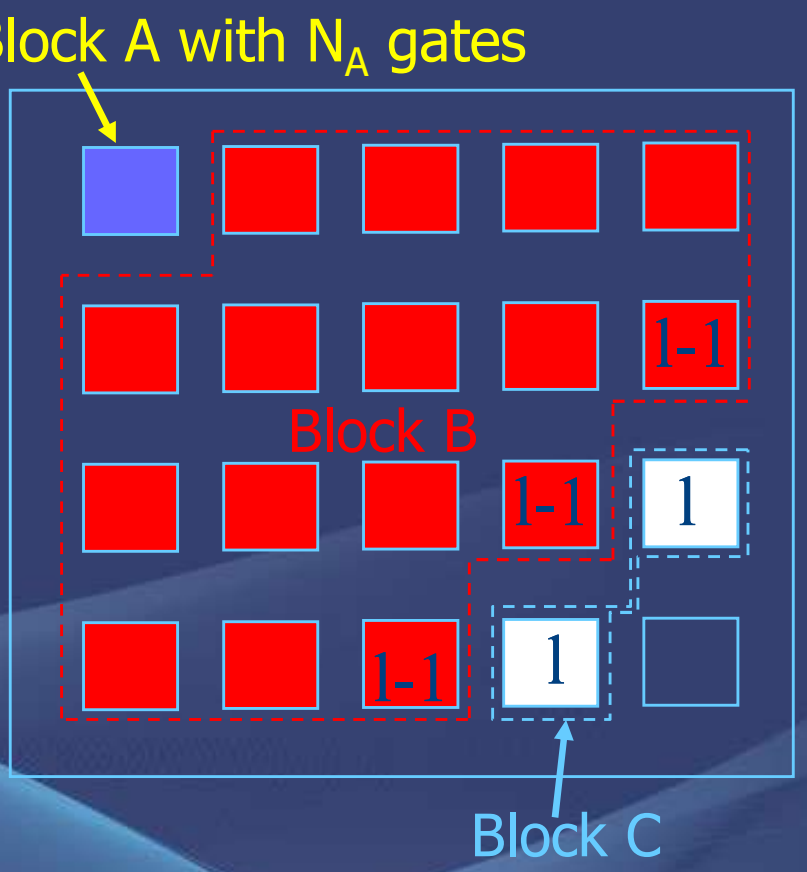
$$T_B + T_C = T_{B\text{-to-}C} + T_{BC}$$

- Values of T within a block or collection of blocks are calculated using Rent's rule, e.g.,

$$T_A = k\,(N_A)^P$$

$$T_{ABC} = k\,(N_A + N_B + N_C)^P$$

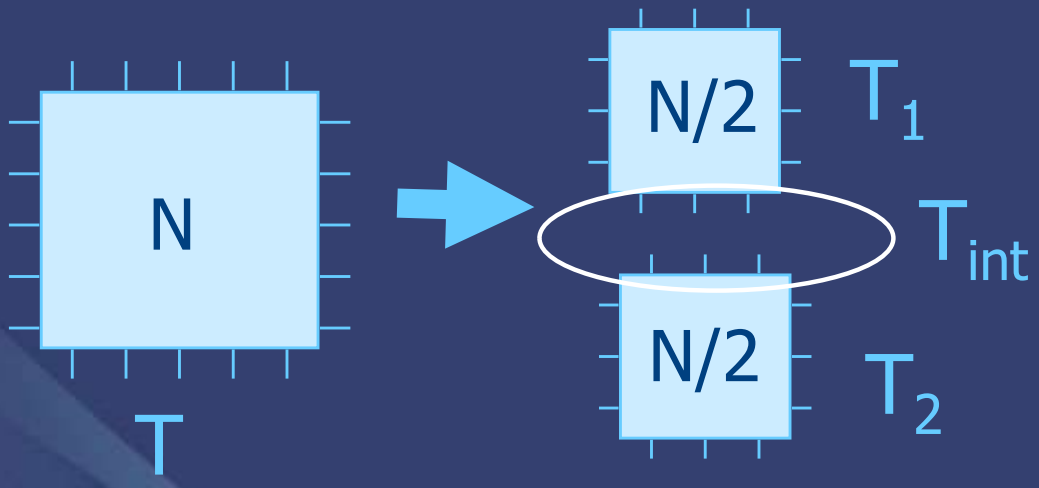
- Recursive use of Rent's rule gives wire-length distribution for the whole chip




Rent's Rule: $T = k N^p$

N = number of gates, k and p denote the average number of fan-out per gate and the degree of wiring complexity (with p=1 representing the most complex wiring network), respectively, and are empirically derived as constants for a given generation of ICs.

# Wire Length Distribution For 3-D ICs



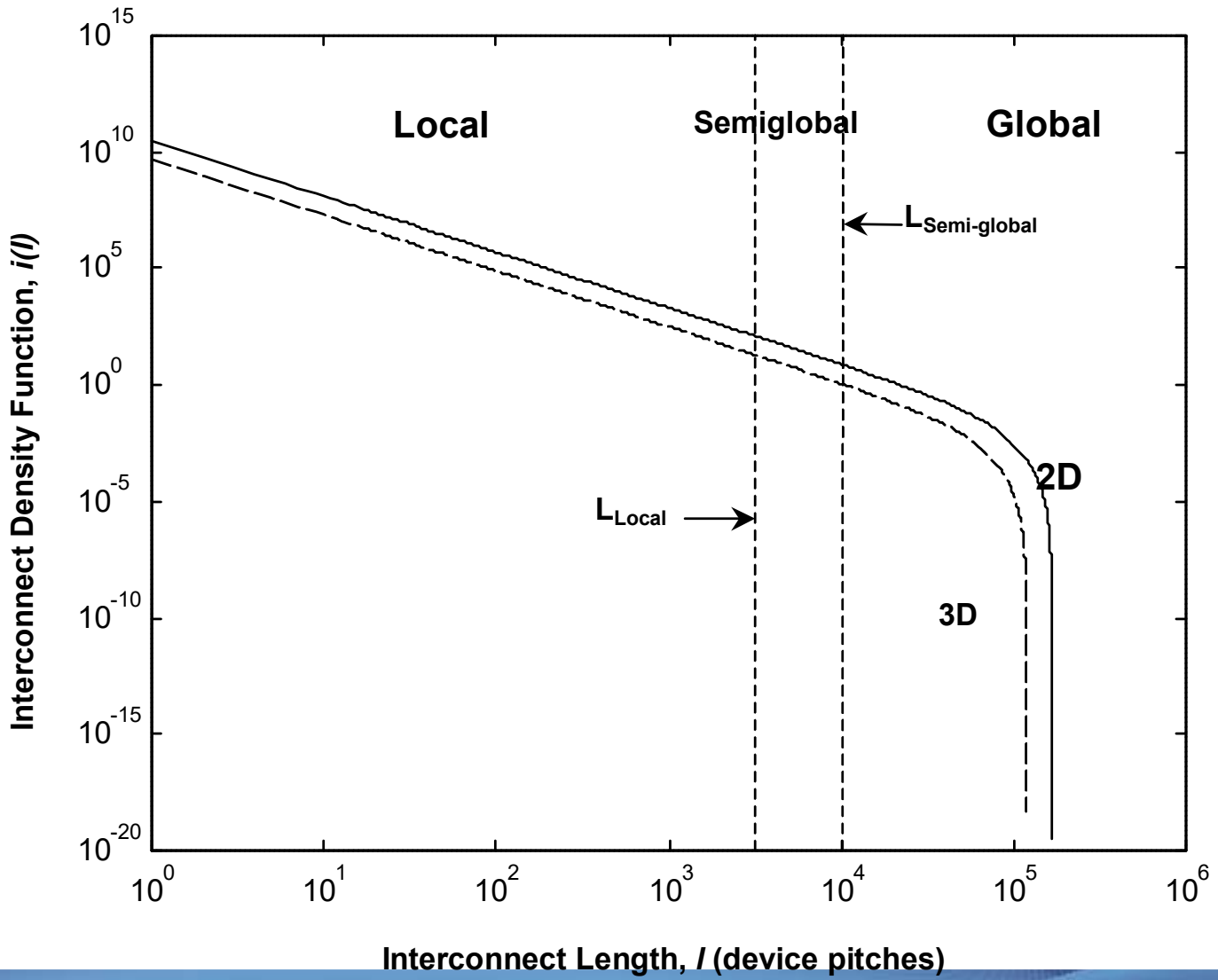

- $T = k N^p = T_1 + T_2 - T_{int}$
- $T_1 = T_2 = k (N/2)^p$
- $T_{ext, i} = T_i - T_{int}/2 = k\, 2^{p-1} (N/2)^p$

For 2 layers:

$k_{eff, ext} = k\, 2^{p-1}$

$k_{eff, int} = k (1-2^{p-1})$

# Wire-Length Distribution

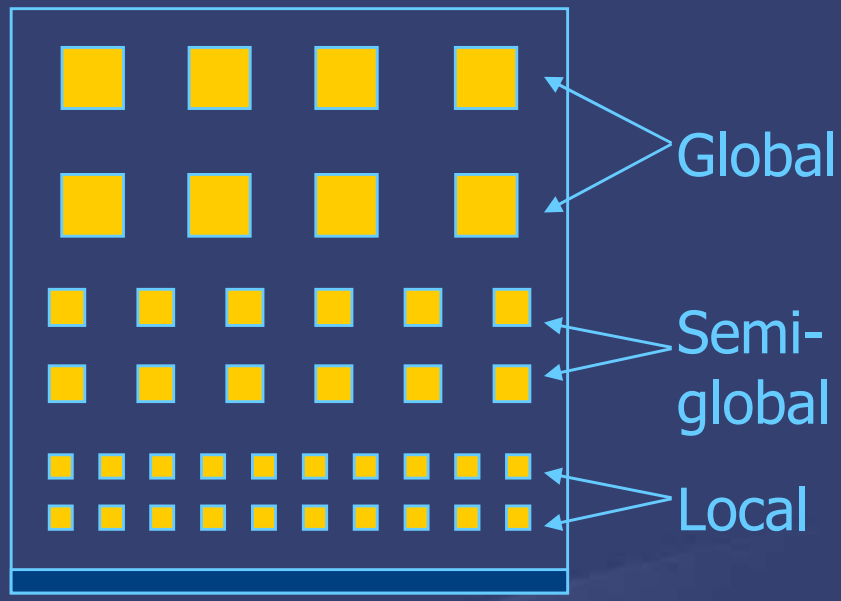



Vertical inter-layer connections reduce metal wiring requirement (50 nm ITRS)

# Chip Area Estimation

- Placement of a wire in a tier is determined by some constraint, e.g., maximum allowed RC delay

A 3-tier wiring network




- Wiring Area = wire pitch x total length

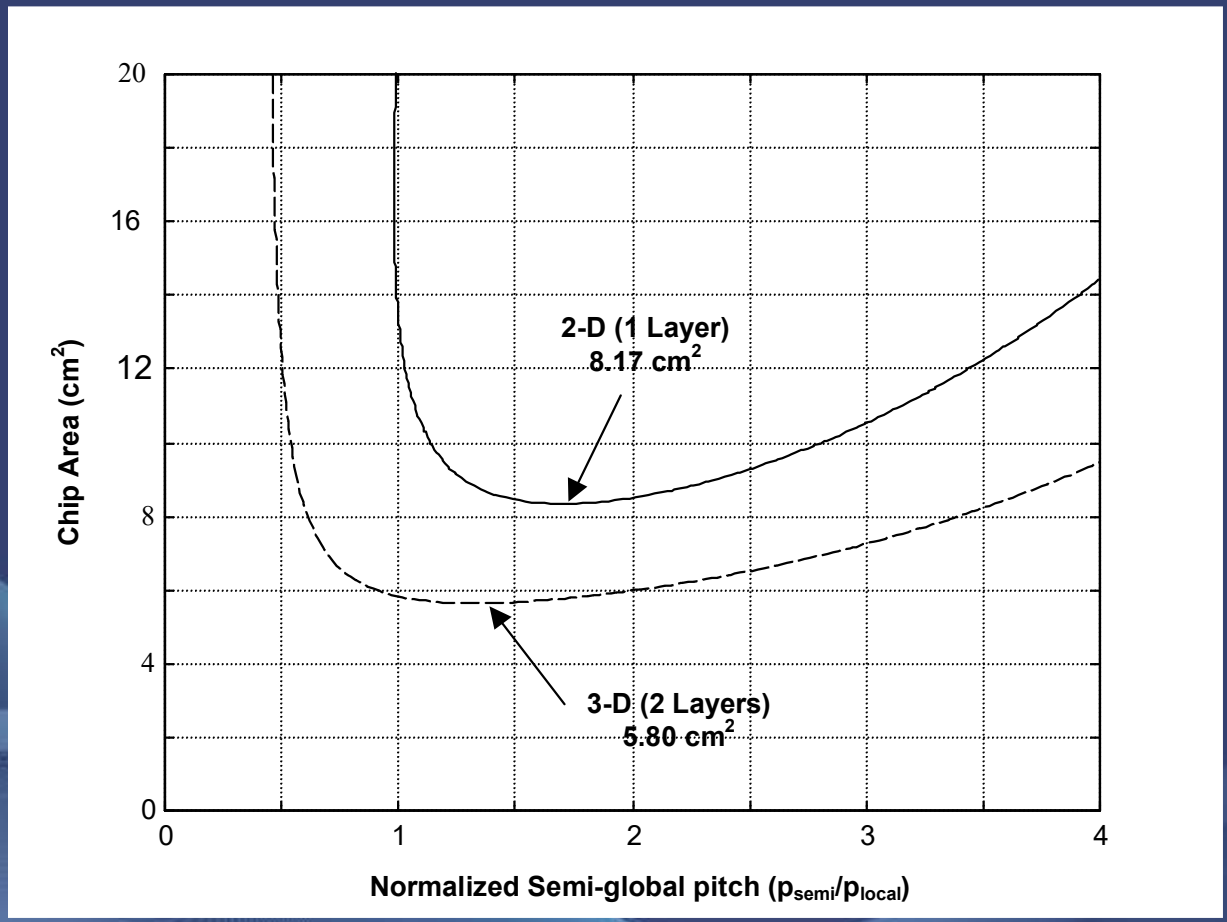
$$A_{req} = p_{loc}L_{tot\_loc} + p_{semi}L_{tot\_semi} + p_{glob}L_{tot\_glob}$$

$$\textit{Chip Area} = \frac{A_{req}}{\textit{\# of Metal Layers}}$$

- $L_{tot}$ calculated from wire-length distribution

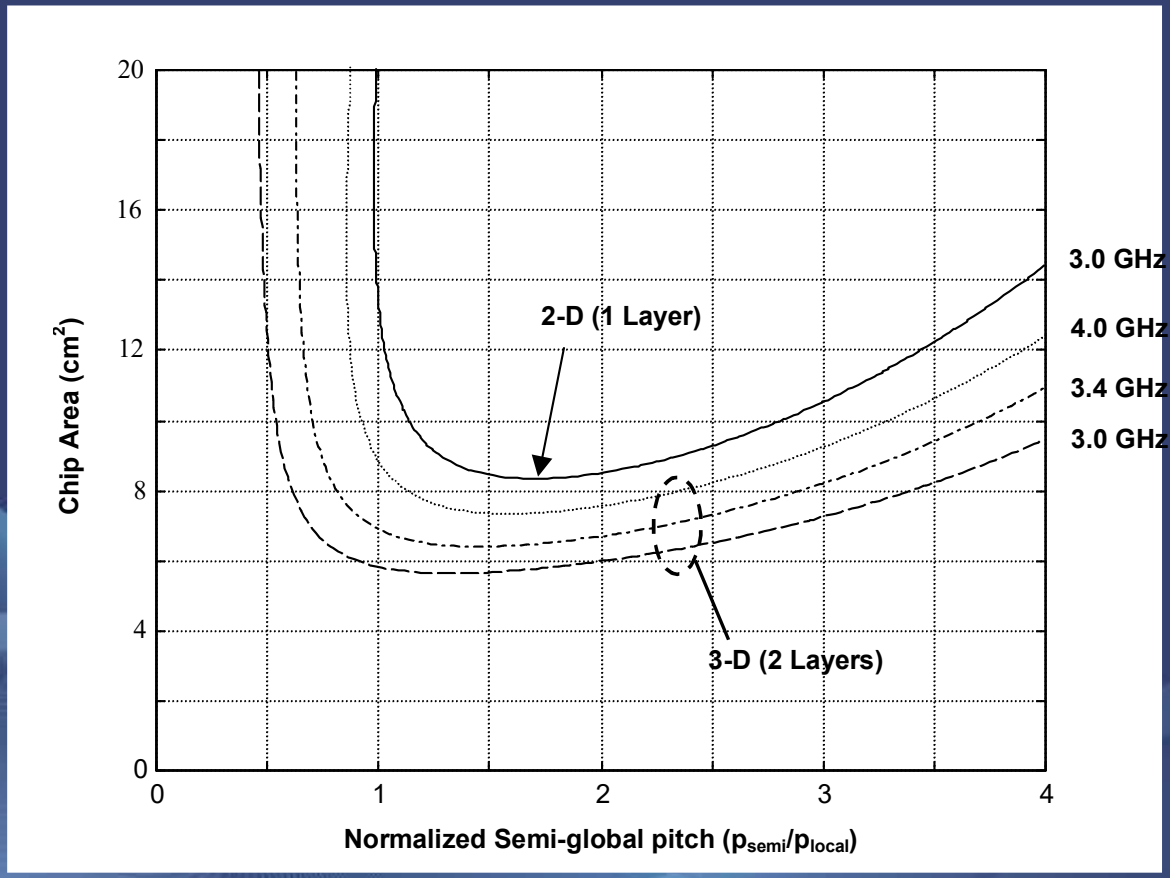
# 2 Active Layer Results

- constant chip frequency, $f_c$
- Less wiring needed
- Around 30% reduction in chip area

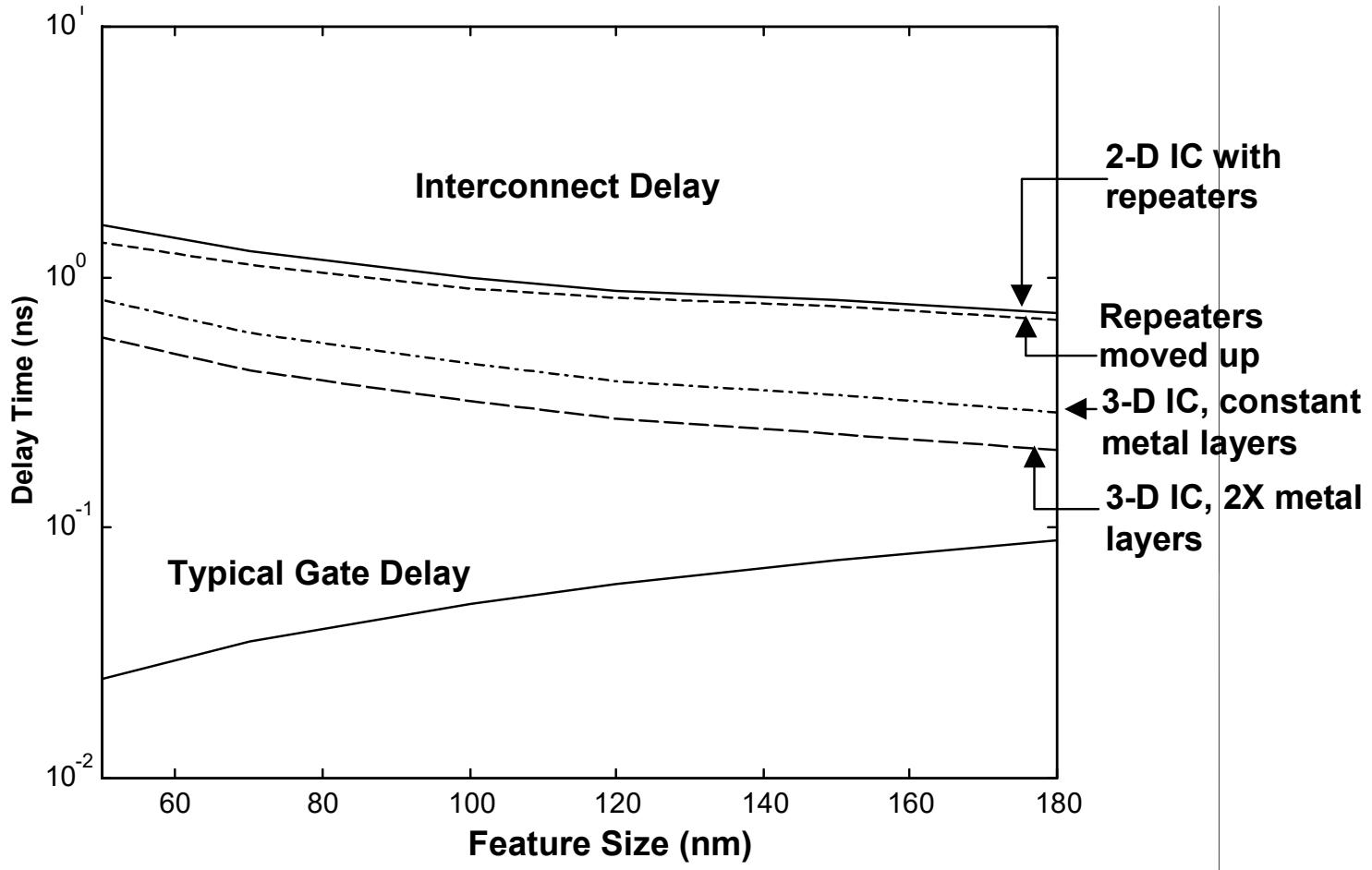


# Improved Performance with Area

- Higher $f_c$ obtained from larger wire pitch
- Results in increase in chip area
- Cannot increase $f_c$ indefinitely



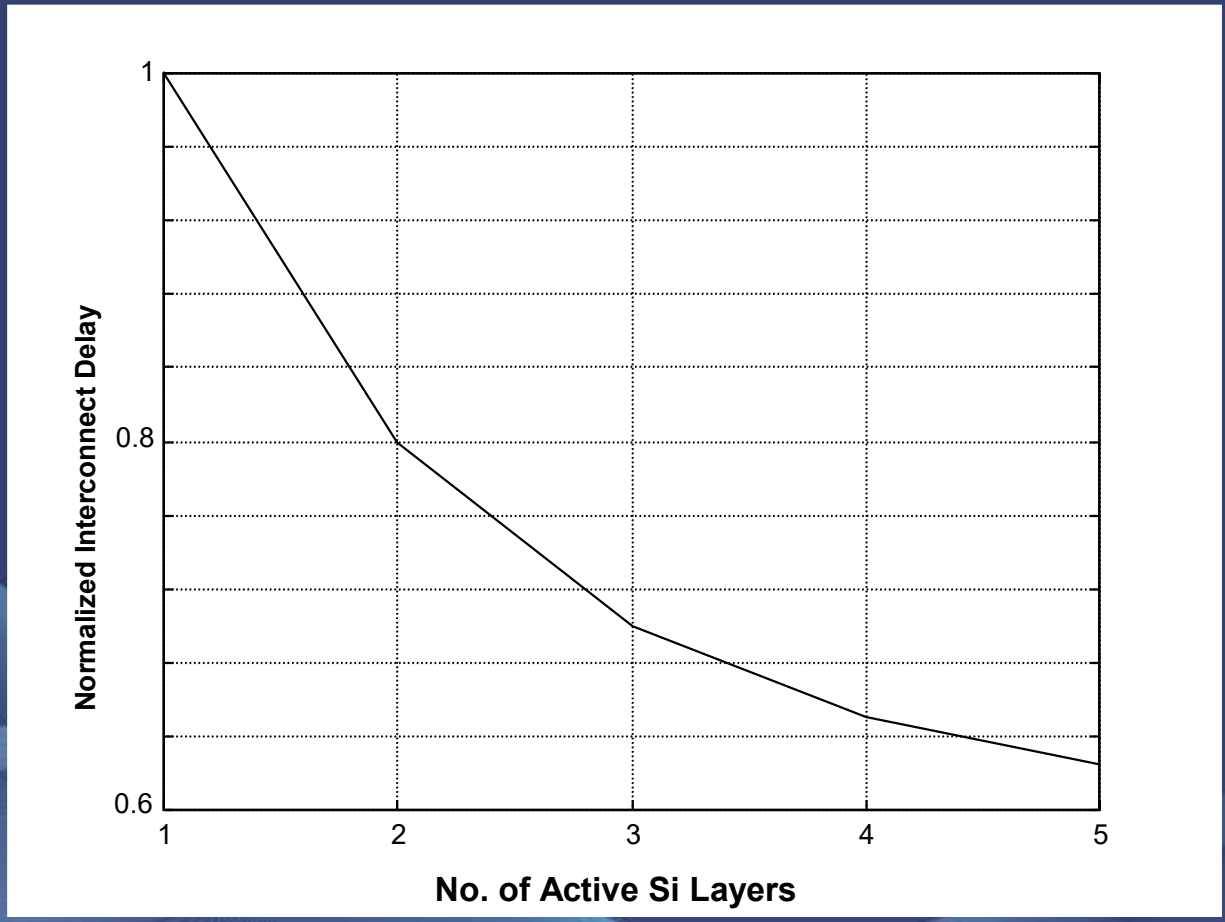
# Performance Summary



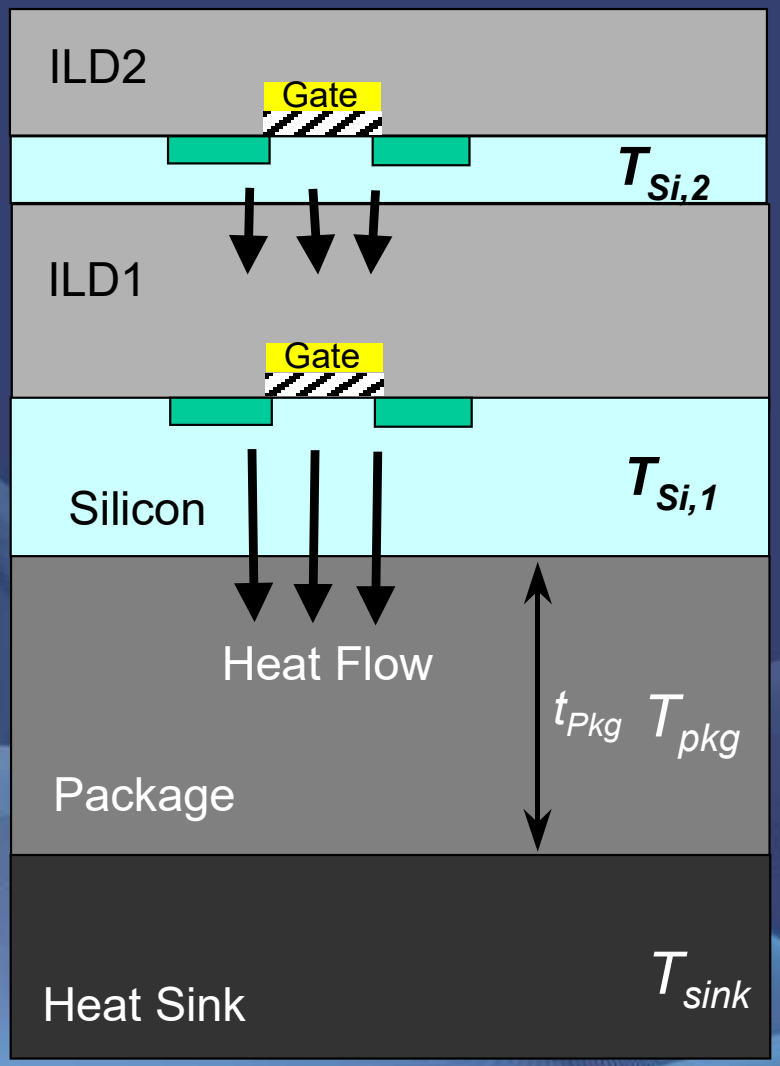

2-Layer 3-D Chip

# More Than Two Active Layers

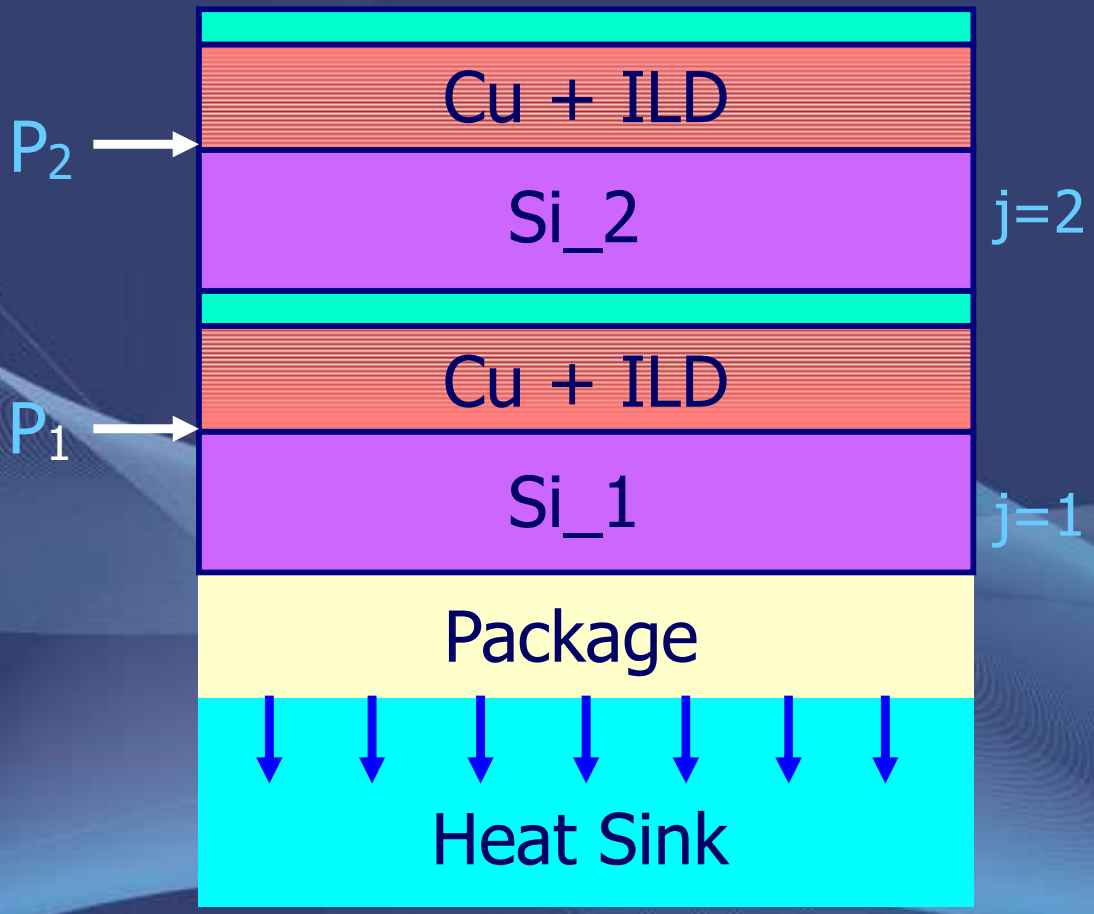
- Simulation based on data from ITRS (50 nm)
- Further improvement in delay achieved



# Thermal Issues



# Analytical Die Temperature Model




- Temperature Rise of the $j^{th}$ Active Layer in an n-layer 3-D Chip

$$\Delta T_j = \sum_{i=1}^{j} \left[ R_i \left( \sum_{k=i}^{n} \frac{P_k}{A} \right) \right]$$

- $n$ = Total Number of Active Layers
- $R_i$ = Thermal Resistance Between Adjacent Layers
- $P_k$ = Power Dissipation in the $k^{th}$ Layer

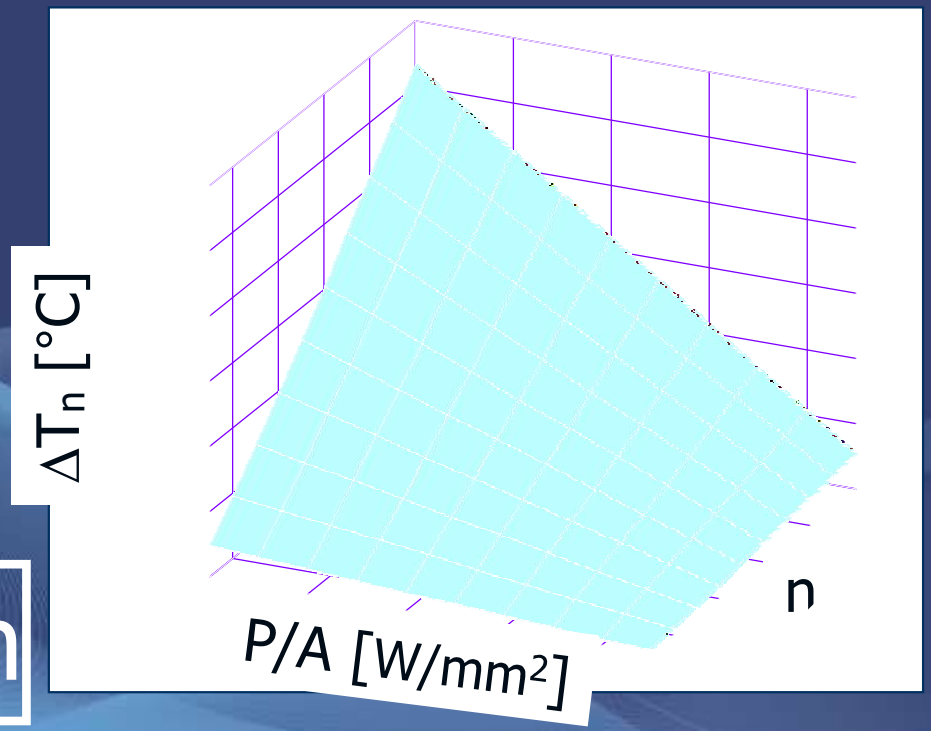
(Im and Banerjee, IEDM 2000)

# Analytical Die Temperature Model

## Temperature Rise of the Uppermost ($n^{th}$) Layer in an n-layer 3-D Chip

$$\Delta T_j = \sum_{i=1}^{j}\left[R_i\left(\sum_{k=i}^{n}\frac{P_k}{A}\right)\right] \longrightarrow \Delta T_n = \left(\frac{P}{A}\right)\left[\frac{R}{2}n^2 + \left(R_1 - \frac{R}{2}\right)n\right]$$

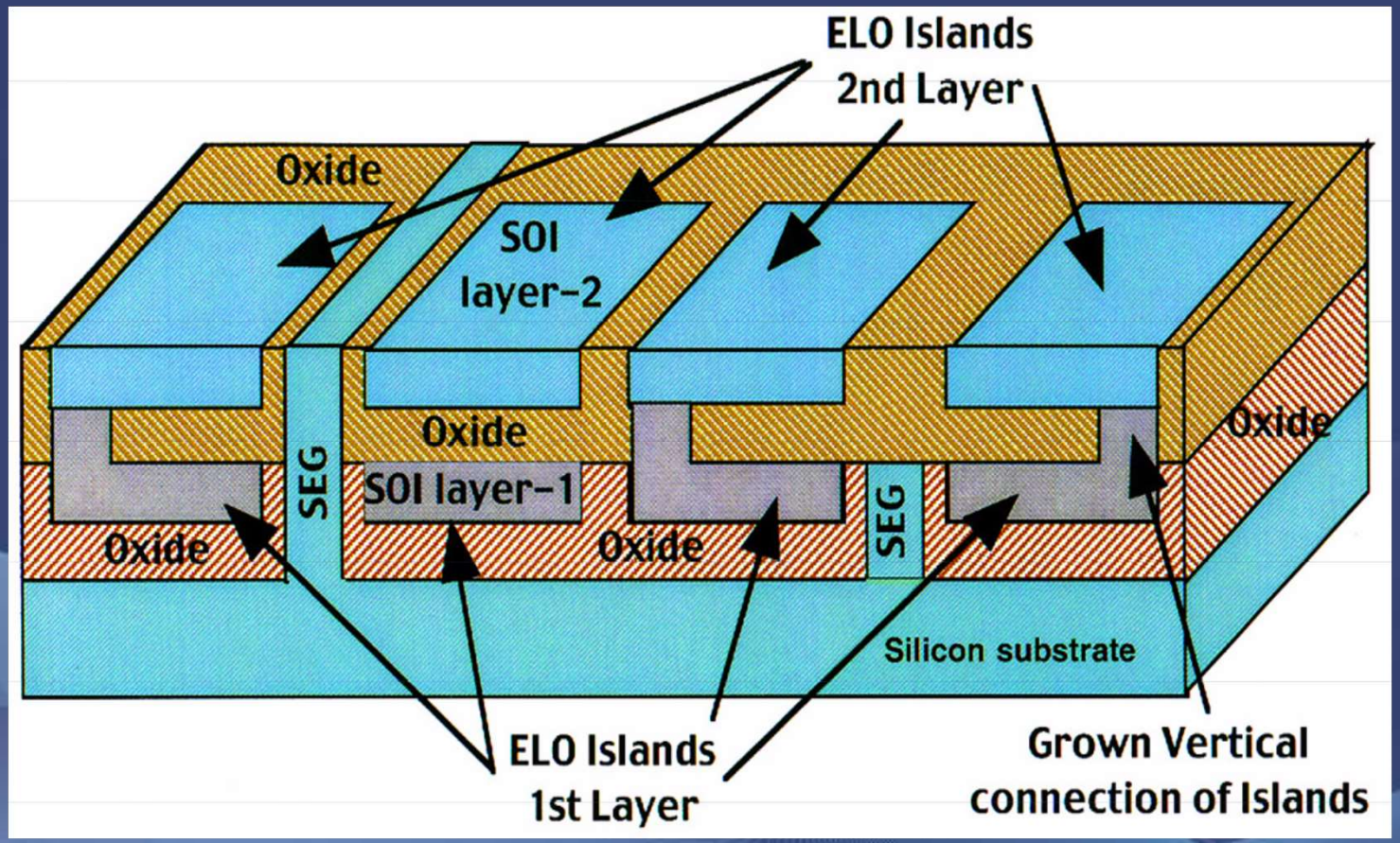
- R = Thermal Resistance Between Adjacent Layers
- $R_1$ = Package Thermal Resistance




- $R_1 >> R$ → Small n → $\Delta T \propto n$

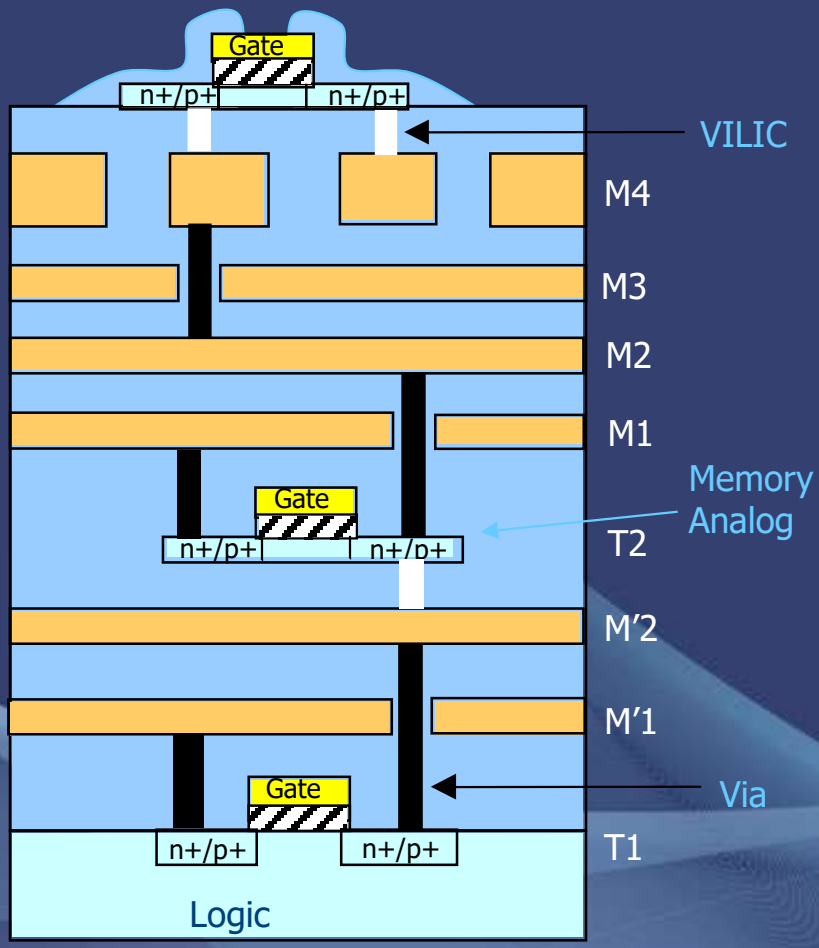
# 3-D Fabrication Technologies

Epitaxial Lateral Overgrowth

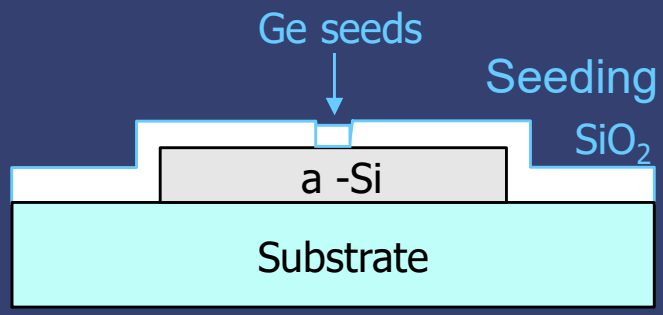


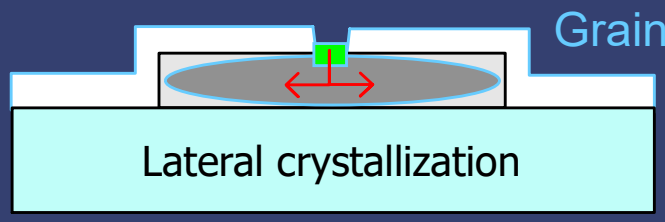

Purdue

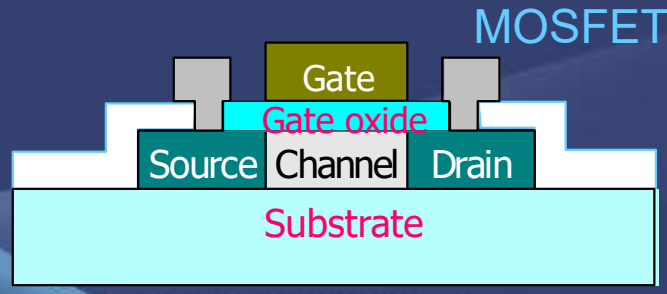
# 3-D Fabrication Technologies




Solid Phase Crystallization of α-Si



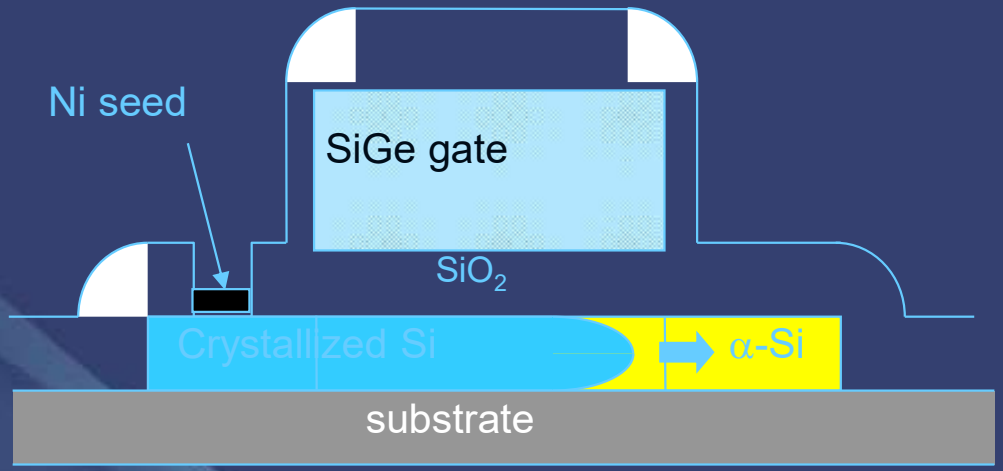




- Locally induce nucleation
- Grow laterally, inhibiting additional nucleation
- Build MOSFET in a single grain with SOI like performance

Stanford

# 3-D Technologies

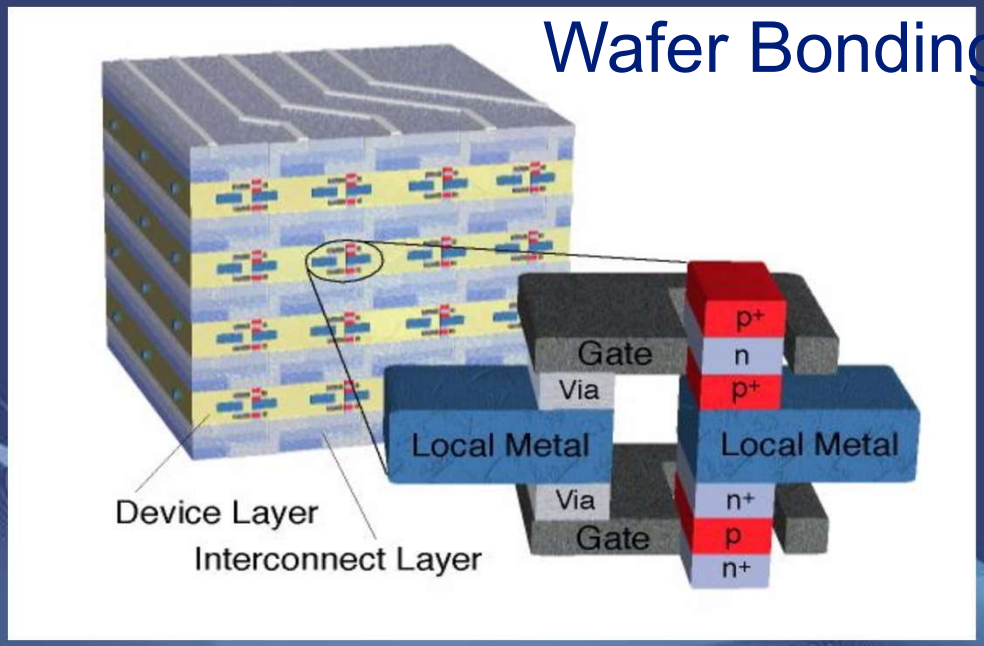
## Ni Seeded Lateral Crystallization




- Initially fabricate amorphous device
- Ni seeding for simultaneous crystallization and dopant activation
- Low thermal budget ($T_{max}$ < 500ºC)
- Devices on top of a metal line
  - MOSFETs
  - Optical detectors

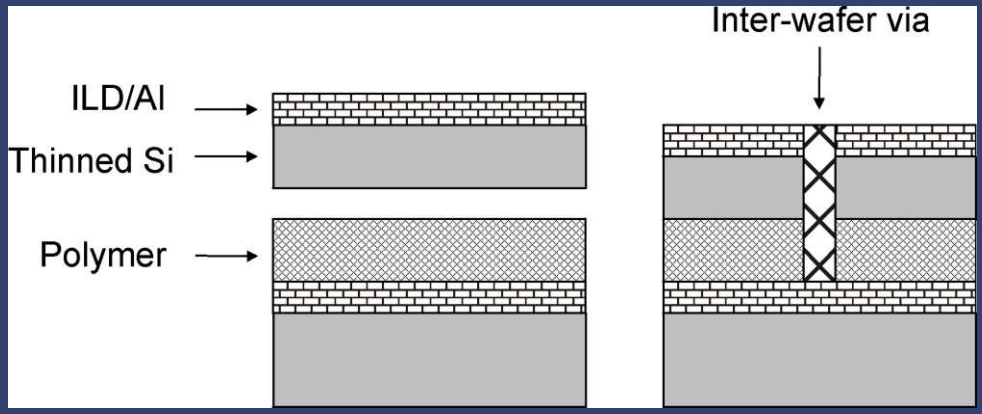
# 3-D Fabrication Technologies

## Wafer Bonding

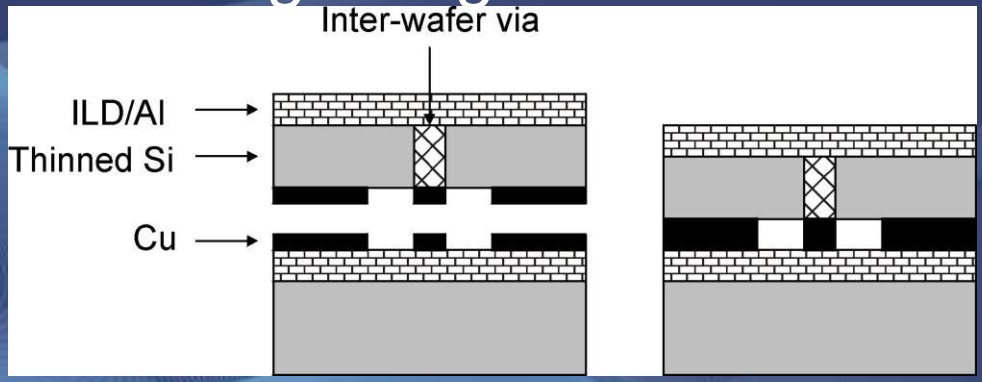



MIT

## Bonding using Glue Layer




## Thermocompression Bonding using Cu Pads



# 3D ICs: Implications for Circuit Design

- Critical Path Layout: By vertical stacking, the distance between logic blocks on the critical path can be reduced to improve circuit performance.
- Repeaters: Some chip area can be saved by placing repeaters (~ 10,000 for high performance circuits) on the higher active layers.

# 3D ICs: Implications for Circuit Design

- Microprocessor Design: on-chip caches on the second active layer will reduce distance from the logic and computational blocks.
- Parallel processor system with three memory layers --multiport memory, overcomes bus bottleneck
- 3-D integration technology --wafer stacking

# 3D ICs: Implications for Circuit Design

- Integration of Disparate Technologies Easier
- RF and Mixed Signal ICs: Substrate isolation between the digital and RF/analog components can be improved by dividing them among separate active layers - ideal for system on a chip design.
- Optical Devices and I/Os can be integrated on the top layer

# 3D ICs: Implications for Circuit Design

- Neuromorphic Vision Chip: Tohoku Univ.

  Achieved an image processing and pattern recognition system with parts of functions of the retina and visual cortex using Si

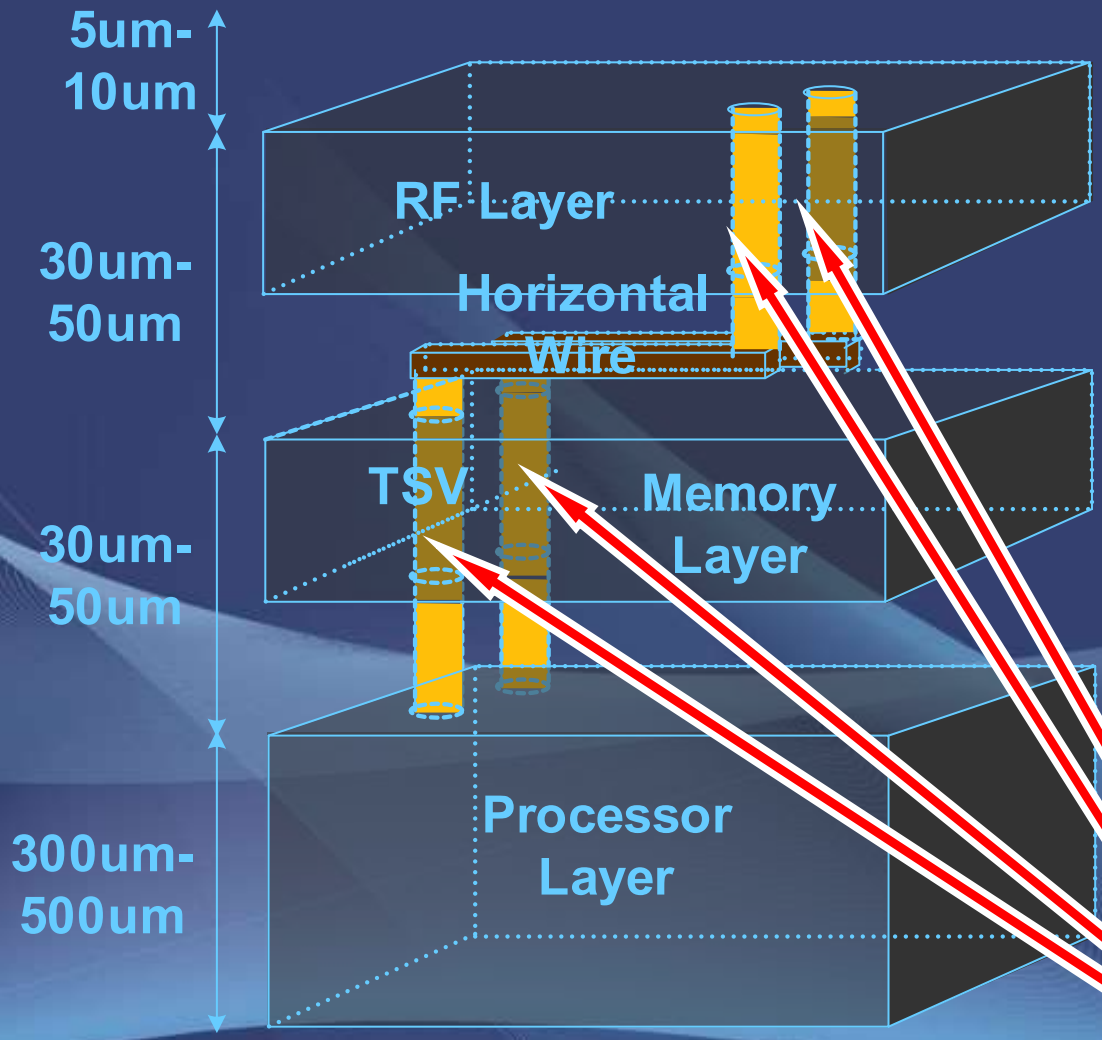
- 3-D Systems-on-a-Chip: MIT, Lincoln Labs

  3D ring oscillators and back-illuminated 64X64 active pixel sensor arrays with fully parallel A/D conversion

- 3-D Assembly Technology: North Corp., Japan

# Compact Modeling of Through-Si Vias (TSV)

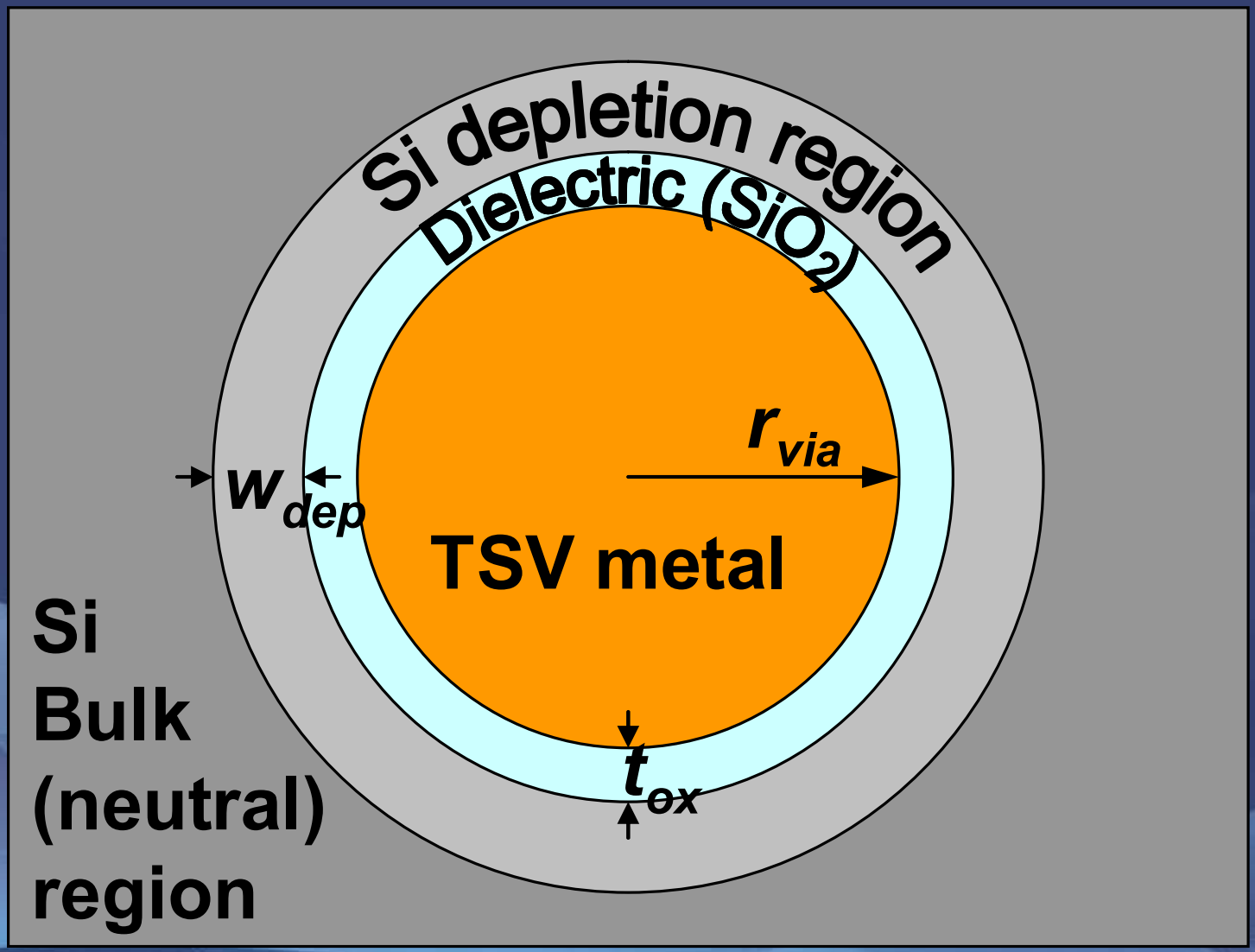
C. Xu, H. Li, R. Suaya and K. Banerjee, IEEE Transactions on Electron Devices, Vol. 57, No. 12, Dec 2010.




- Increase functionality, performance and integration density…
- "More-than-Moore" technologies

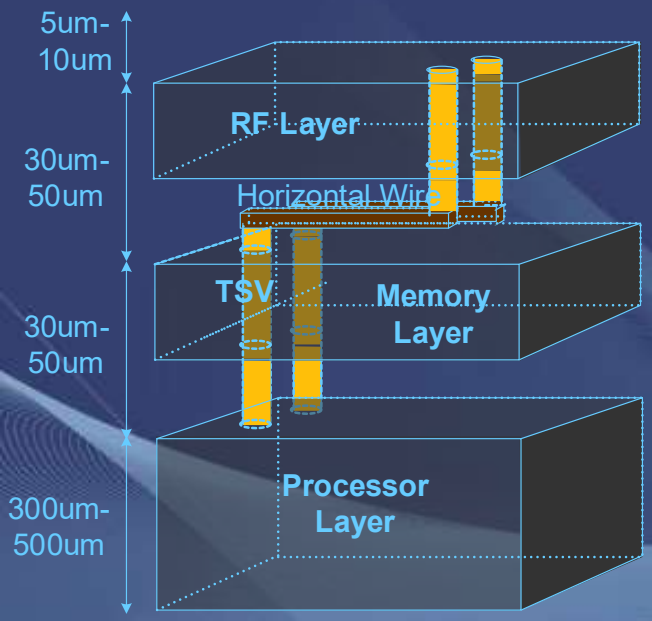
TSVs – Connections between layers

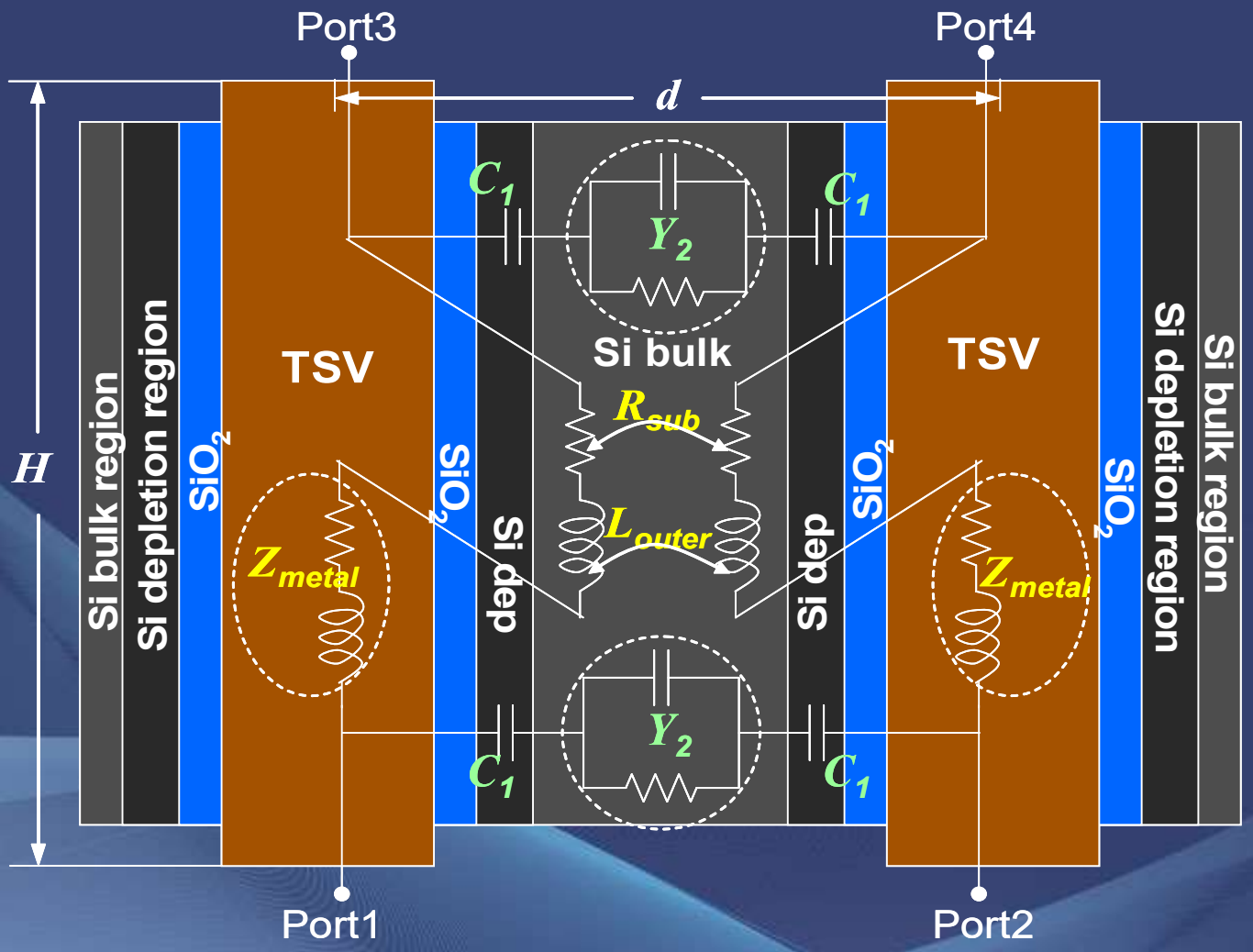
# Top Cross-Sectional View of a TSV



# Compact TSV Modeling for 3-D ICs

- High aspect ratio (>10)
- Long lengths (20-100 μm)

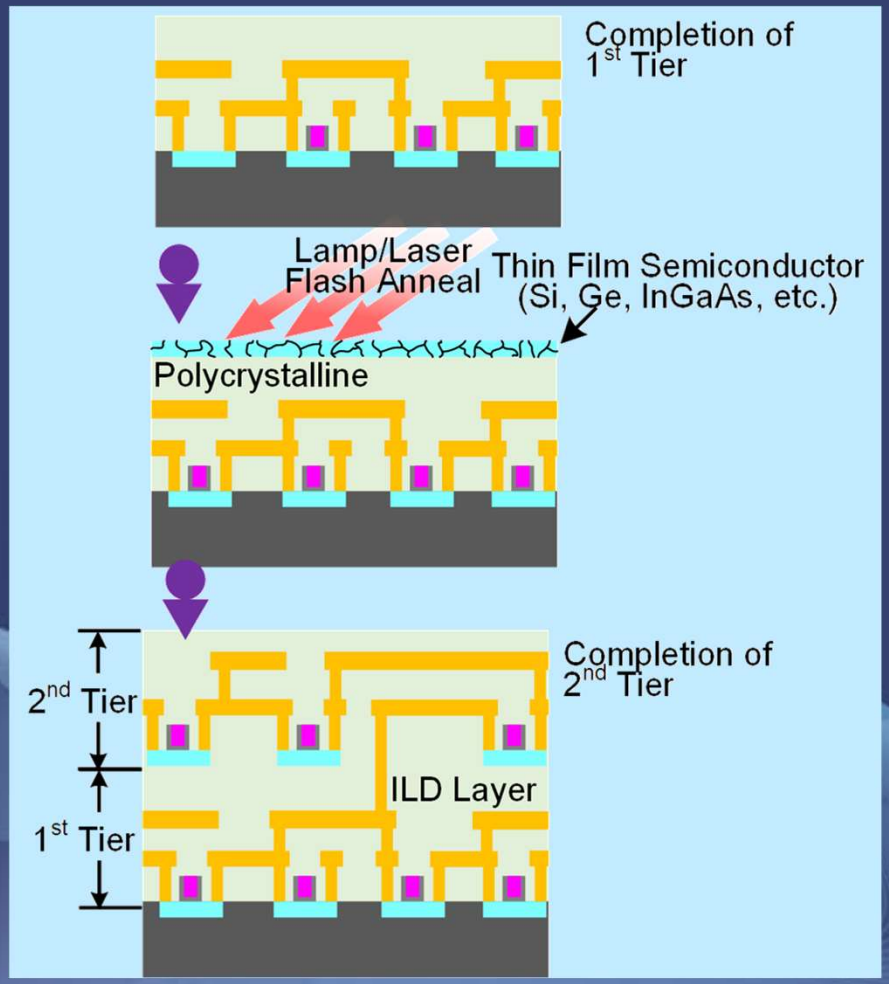



- RLGC transmission line model: with consideration of depletion region, AC conduction and eddy current effect
- $C_1$ accounts for the electrostatics, $Y_2$ accounts for the conductance and capacitance of bulk Si, $Z_{metal}$ accounts for the inner impedance of the TSV-metal, $L_{outer}$ and $R_{sub}$ are due to the outer impedance of the TSV-pair

# Ultimate Monolithic-3D Integration with 2D Materials

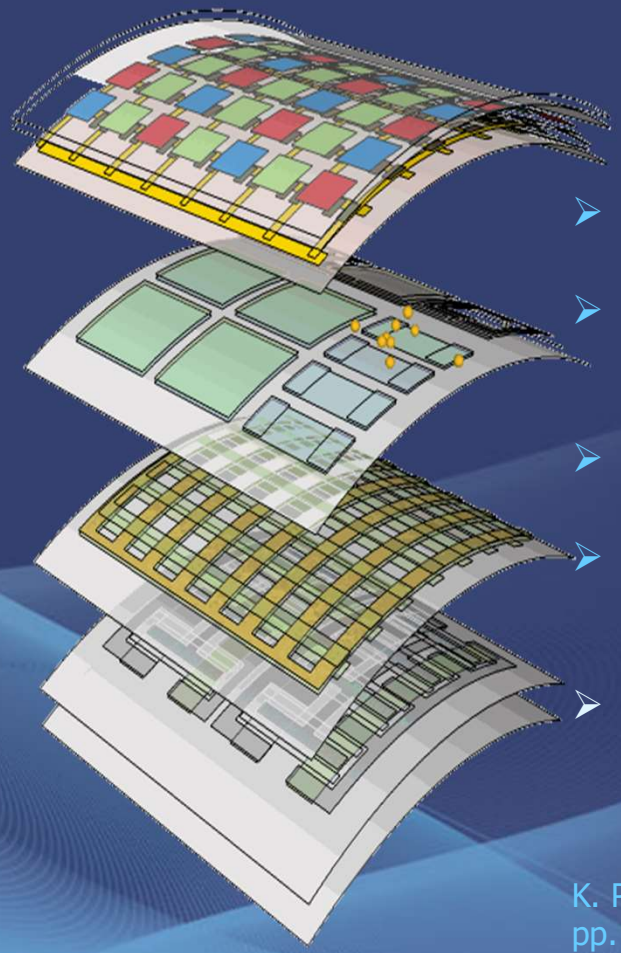
## Current Monolithic 3D Solution




- Hard to grow high-quality semiconducting layer under process thermal budget
- Thick tiers results in large inter-tier signal delays and thermal resistance

J. Kang et al., ***Proc. SPIE***, 9083, 908305, 2014.

## Hybrid Integration of 2D Electronics



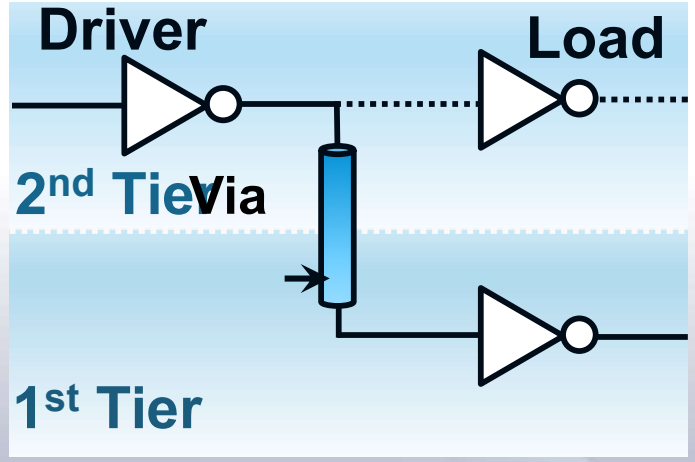
- **Low-T deposition of 2D**
- **Thinner body - lower thermal resistance**
- **Improved lateral heat dissipation**
- **Higher integration density**
- **Interfaces dominate thermal transport…**

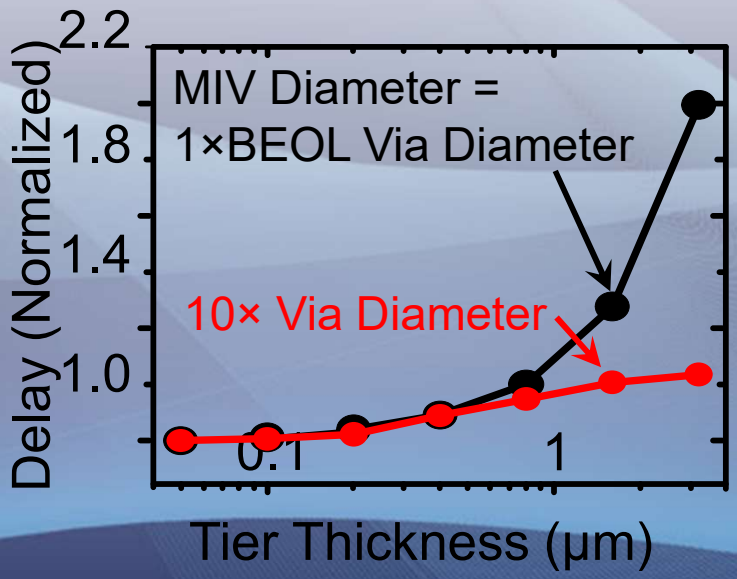
K. Parto et al., ***IEDM*** 2018, pp. 24.1.1-24.1.4

J. Jiang, K. Parto, W. Cao & K. Banerjee ***IEEE J-EDS***, vol. 7, 2019

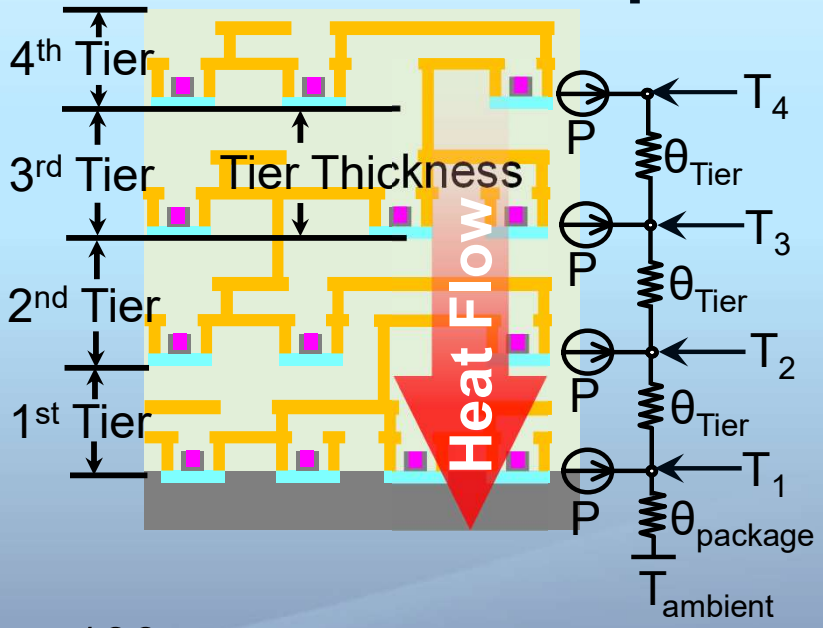
# Monolithic 3D Integration with 2D Materials – Motivation

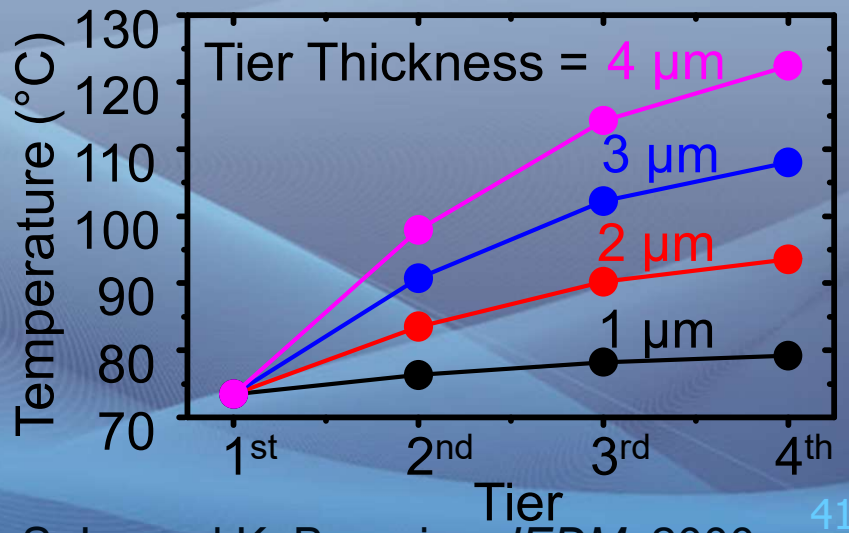
## Inter-Tier Signal Delay



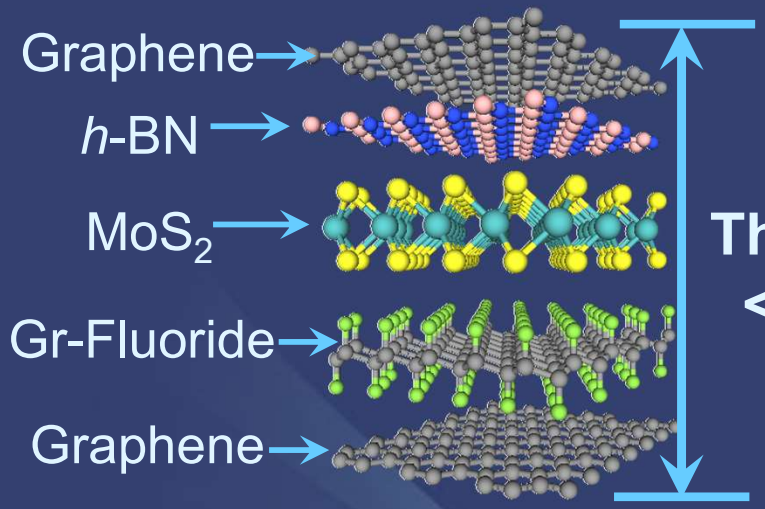

## Vertical Heat Dissipation

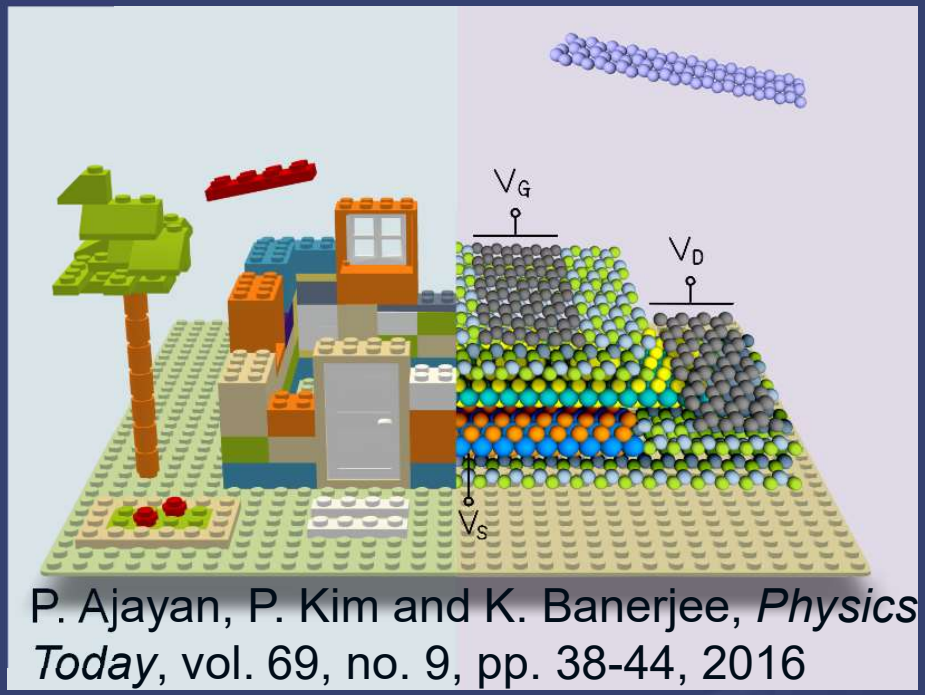



S. Im and K. Banerjee, *IEDM*, 2000.

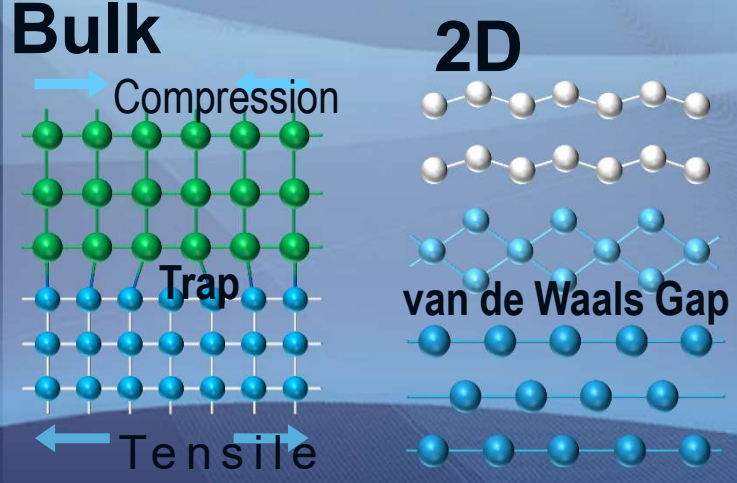
# 3D Integration with 2D Materials

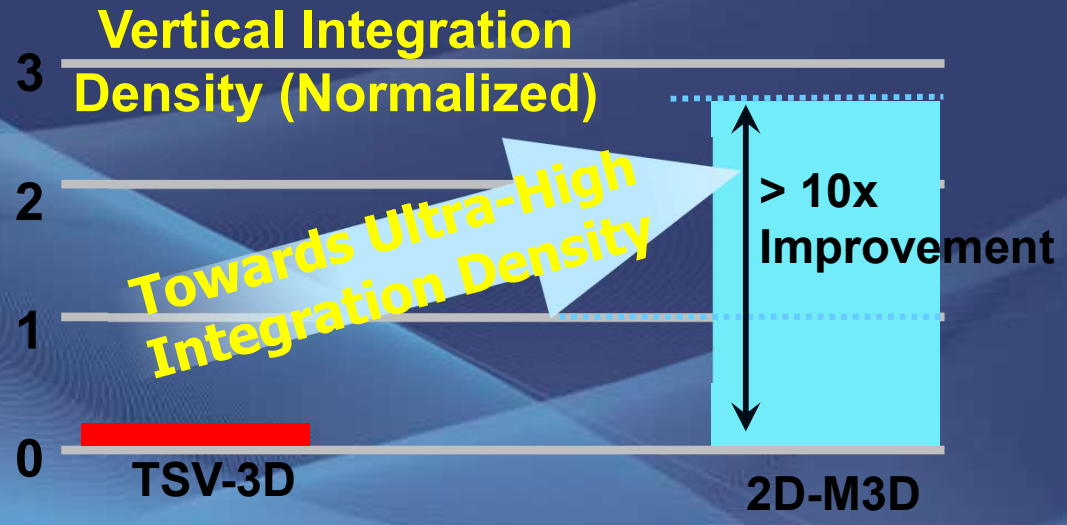



P. Ajayan, P. Kim and K. Banerjee, *Physics Today*, vol. 69, no. 9, pp. 38-44, 2016

vdW Interface in 2D Stackings
→ No Lattice Mismatch
→ Stress Free



# A Novel Memory Cell Specifically Suited for Ultimate Monolithic-3D Integration….

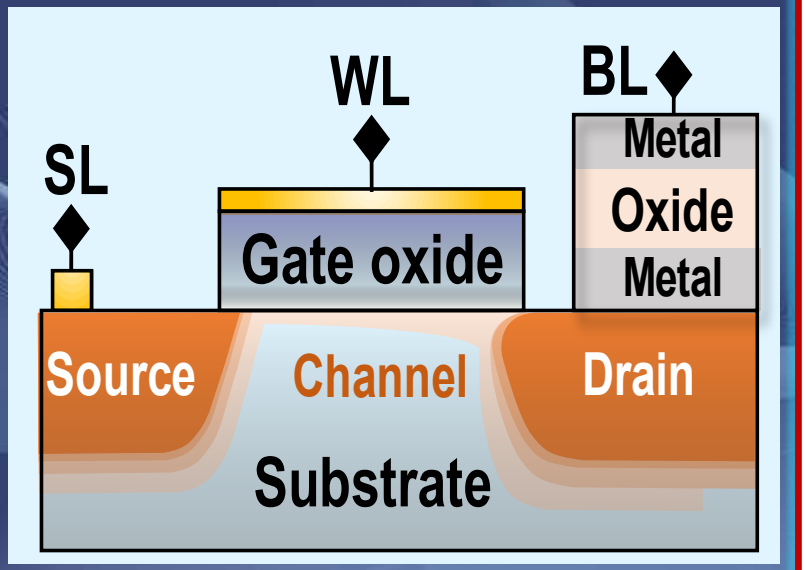
## 0.5T0.5R – A "Smart" Transistor with Embedded RRAM

**First ever in RRAM technology history…**

**Excellent hardware platform for neuromorphic and in-memory computing**

D. Zhang et al., ***IEEE TED***, vol. 68, no. 4, pp. 2033-2040, 2021.

**Conventional 1T-1R RRAM**

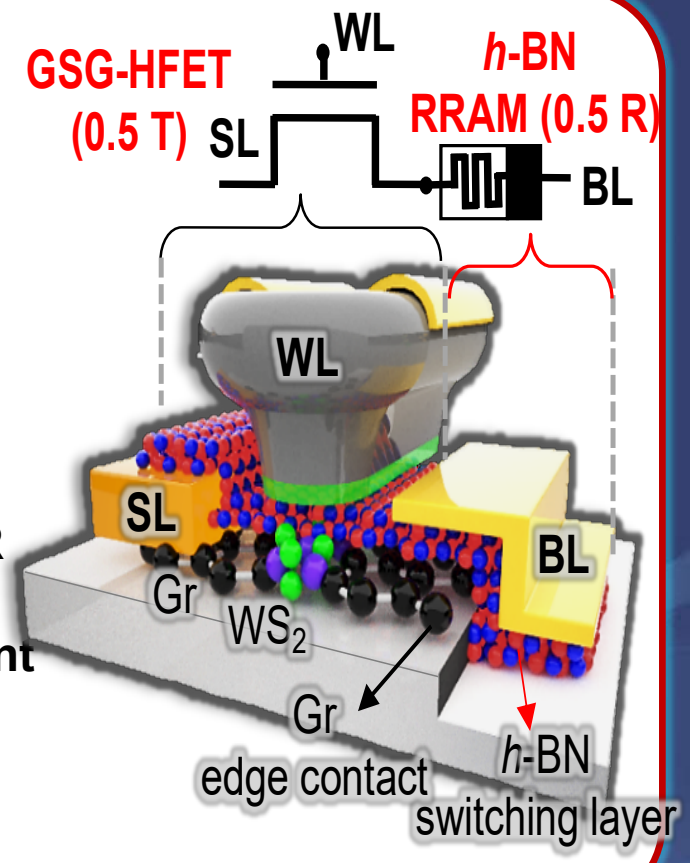



**0.5T0.5R**

**Gr-$WS_2$-Gr HFET + *h*-BN RRAM**

**Key features:**

- **Integrates 1T and 1R into a single device**
- **Reduces device count by half**
- **Higher lateral and vertical integration density**



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# Transistors and memory get together

Stuart Thomas

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*IEEE Trans. Electron Dev.* **68**, 2033–2040 (2021)

0.5T0.5R Cell Array