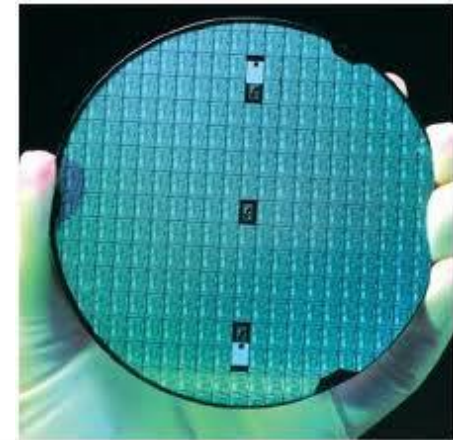
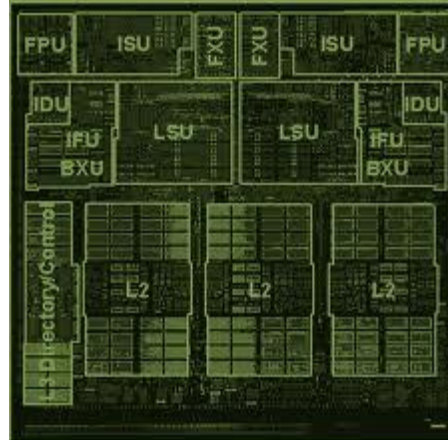
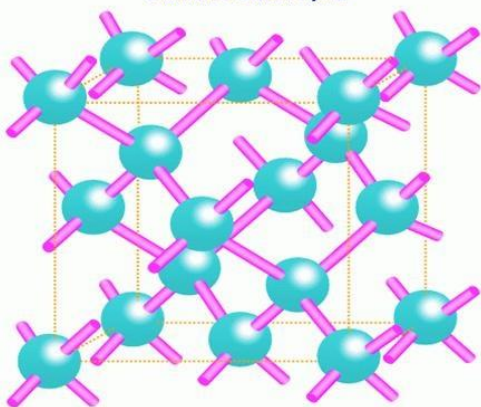


Structure of silicon crystal



ECE 225

High Speed Digital IC Design

Lecture 2

Discussion of Project Topics

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Electrical and Computer Engineering
University of California, Santa Barbara
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Suggested Project Topics....

- **Emerging Technologies for VLSI and More-than-Moore Technologies:** **issues relevant to circuit design/optimization**
 - a. Si-based – FinFET, GAAFET, stacked-Nanowire/Nanosheet- FET
 - b. Non-Si – such as 2D-FETs, CNT-FETs, etc
 - c. Memory technologies - new designs for SRAM/DRAM/Flash
 - RRAM, MRAM, FRAM, STT-RAM, PCM etc
 - d. Energy-efficient devices – TFETs, IMOS, Fe-FET, NEMFET, IMT, etc.
 - Non-charge (spin) based devices
 - e. Monolithic 3D ICs: design architectures for maximizing performance and energy-efficiency, opportunities with new materials and devices
 - f. Emerging interconnect technologies: nano-carbons such as graphene nanoribbons, optical, RF interconnects etc
 - g. On-chip inductors/capacitors (materials, mechanisms, designs...)
 - **Non-Von Neumann Architectures**
 - a. Neuromorphic computing (materials, devices, circuits...)
 - b. In-Memory computing
- Note: The listed topics above are suggestions only. You may choose a topic outside of this list, but prior approval is needed.***

Project Timeline....

- ❑ Must work individually...
- ❑ Topic/Abstract due: Jan 21 (~ 200-300 words)
 - Literature review and identify problem to be addressed within a given topic.
 - Justify your project...
- ❑ Final project presentations: toward the end of the quarter (~25 mins per student)
- ❑ Final project report due in March (end of finals week)



66th
International
Electron
Devices
Meeting

0.5T0.5R – A “Smart” Transistor with Embedded RRAM

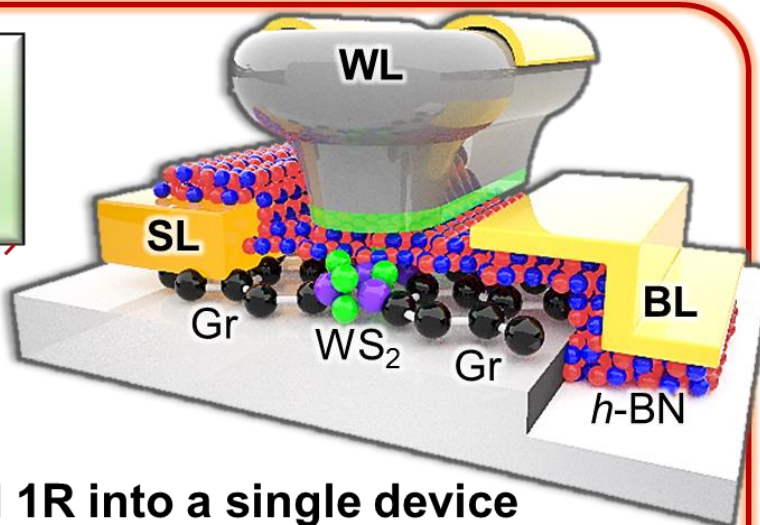
Paper #: 12.3 (Tuesday, Dec 15, 2020)

First ever in RRAM technology history...

Excellent hardware platform for neuromorphic and in-memory computing

0.5T0.5R

Gr-WS₂-Gr HFET +
h-BN RRAM



Key features:

- Integrates 1T and 1R into a single device
- Uniquely enabled by 2D materials
- Reduces device count by half
- Enables neuromorphic and in-memory computing

0.5T0.5R Hybrid Device

- Ultra-compact footprint
- Access latency:
< 10 ns
- Programming energy:
0.07 pJ/bit