University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #2

Due Date: March 10th, 11:59 pm via GradeScope

Question 1 – Tunneling FETs (20 pts)

Please review lecture 9, slide 13 showing the slow V_{ds} turn-on.

a) Why the I_D-V_D is not linear at low V_D regime? Is this an intrinsic or extrinsic property? Is there any possibility to eliminate it? If tunnel FETs are used to design a 1T-DRAM, what effect could be expected?

b) Analyze the enhanced Miller effect in a tunnel FET based inverter with load capacitance, reproduce the figure (showing Miller effect) by SPICE simulation. (hint: you can use MOSFETs instead of tunnel FETs in the simulation, and artificially change the capacitance).

Question 2 – Minimum V_{DD} for Different Logic Styles (20 pts)

The minimum supply voltage (V_{DD}) for a static CMOS inverter gate was discussed and derived in class. Using similar approach, derive the minimum VDD for the following inverter logic styles:

a) Pseudo-NMOS
b) Resistive load inverter
c) Pass-transistor logic
d) Dynamic gate.

Discuss all possible cases and state any assumptions. Partial credit will be given based on your efforts.

Note: You may supplement your analytical solutions with SPICE simulations to provide additional support.

Question 3 – Three-Dimensional Integration (20 pts)

Read the article to be posted under the Lecture "3D Integrated Circuits", by *Banerjee et al.*, *Proceedings of IEEE, 2001*, and answer the following questions.

1. What are the benefits of 3D integration?

2. Prepare a table summarizing various 3D ICs introduced so far by commercial entities and their timelines. What is the total 3D IC market (in billions of dollars) and what are the projections?

3. What are the current 3D IC fabrication methods? List the various challenges?

4. What are the benefits of monolithic 3D integration? Why are 2D materials beneficial for monolithic 3D integration?

Question 4 – Device Variations and Novel Keeper Gate Design (20 pts)

a) In the paper titled "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic OR gates" by H. Dadgour, briefly explain what the motivation for the keeper circuit is.

b) Explain how the process variation sensor circuit works.

c) What do you think the major sources of variation in devices are? Among one of the important sources of variations discussed, the gate metal work-function is one of them. Explain the reasons behind the difference in metal work-function for difference grain orientations. Why is this more important in smaller channel length transistors?

Question 5 – Non-conventional memory technologies (20 pts)

Summarize the scaling challenges for different types of memories, including **SRAM**, **DRAM**, **flash memory**, **3D-NAND**, **memristor**, **Phase Change Memory (PCM)**, **Spin Torque Transfer Magnetic Memory (STT-MRAM)**, **Resistive Memory (RRAM)**, **Conductive-bridging Memory (CBRAM)** and **Ferroelectric RAM (FeRAM)**. Discuss the advantages and disadvantages of these emerging memory technologies in different applications.