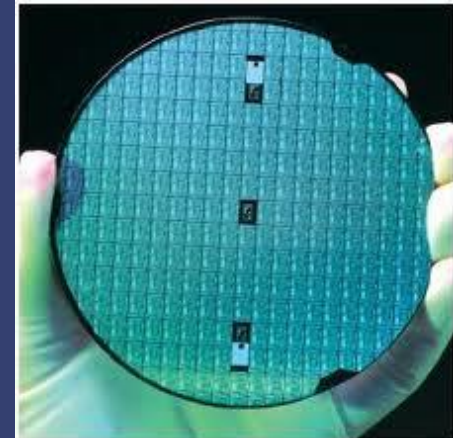
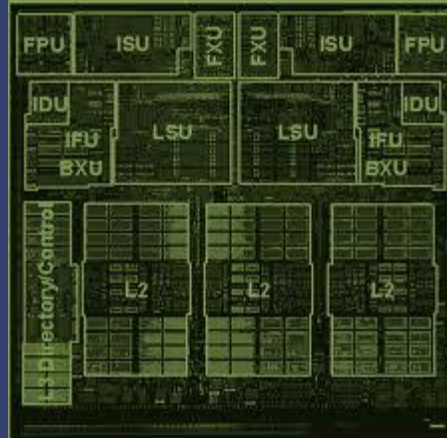
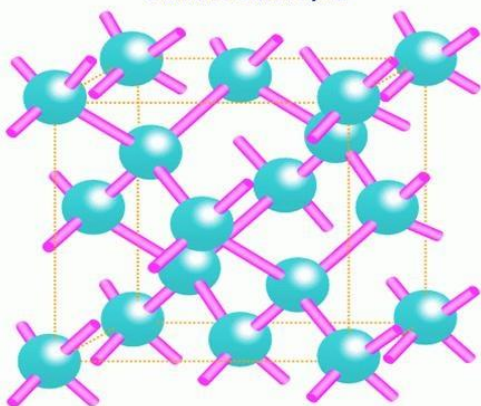


Structure of silicon crystal



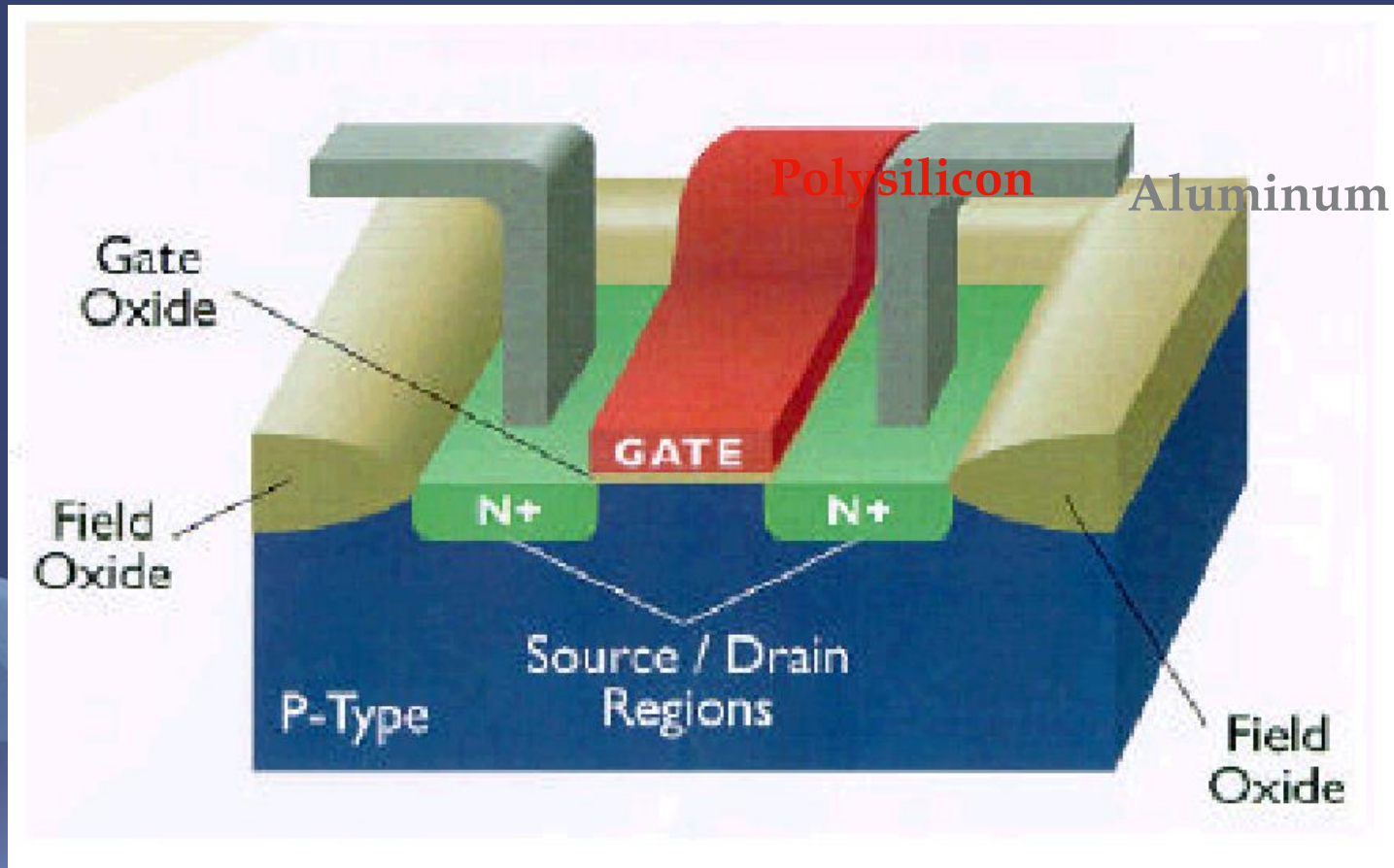
ECE 225

Lecture 8

Non-Classical CMOS Devices

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara

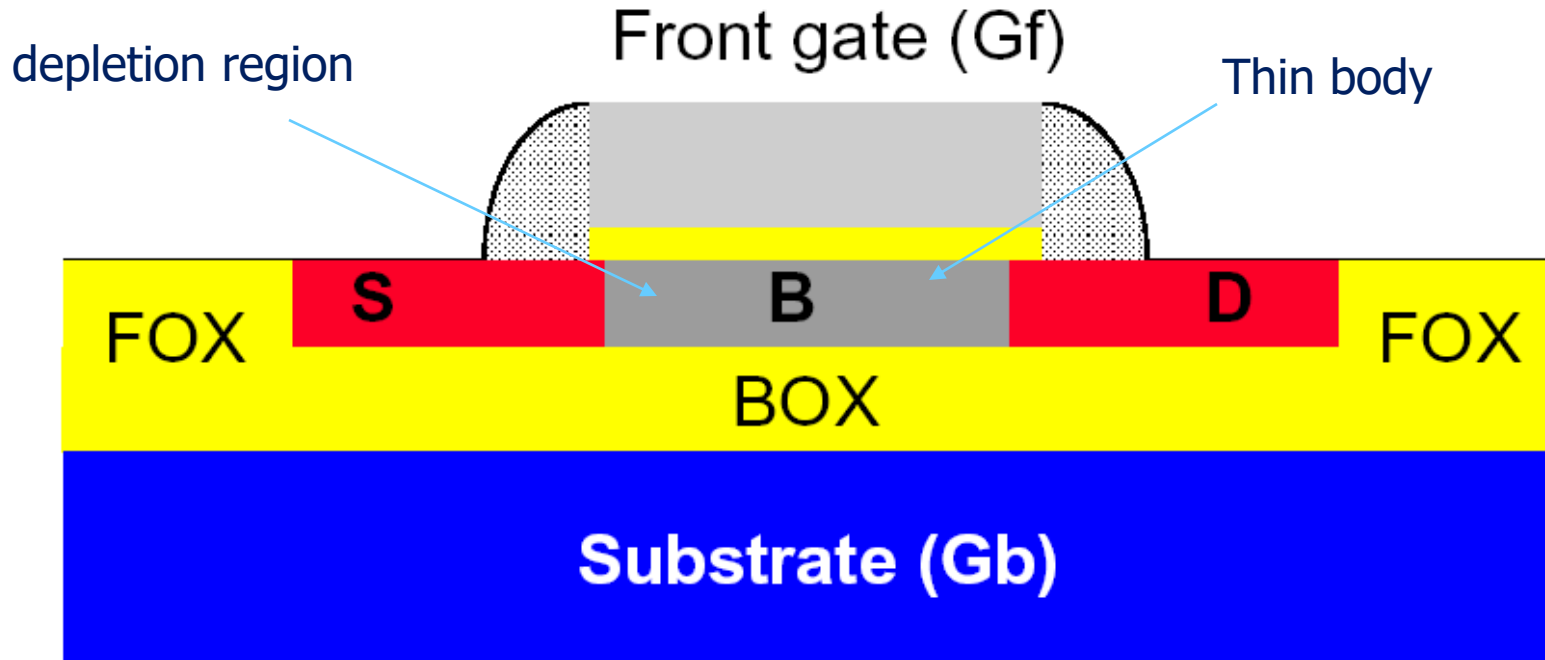
Classical MOSFET Structure



3D Schematic of a n-type MOSFET

Non-classic CMOS Devices

basic structures



Fully depleted (FD) body

Another View

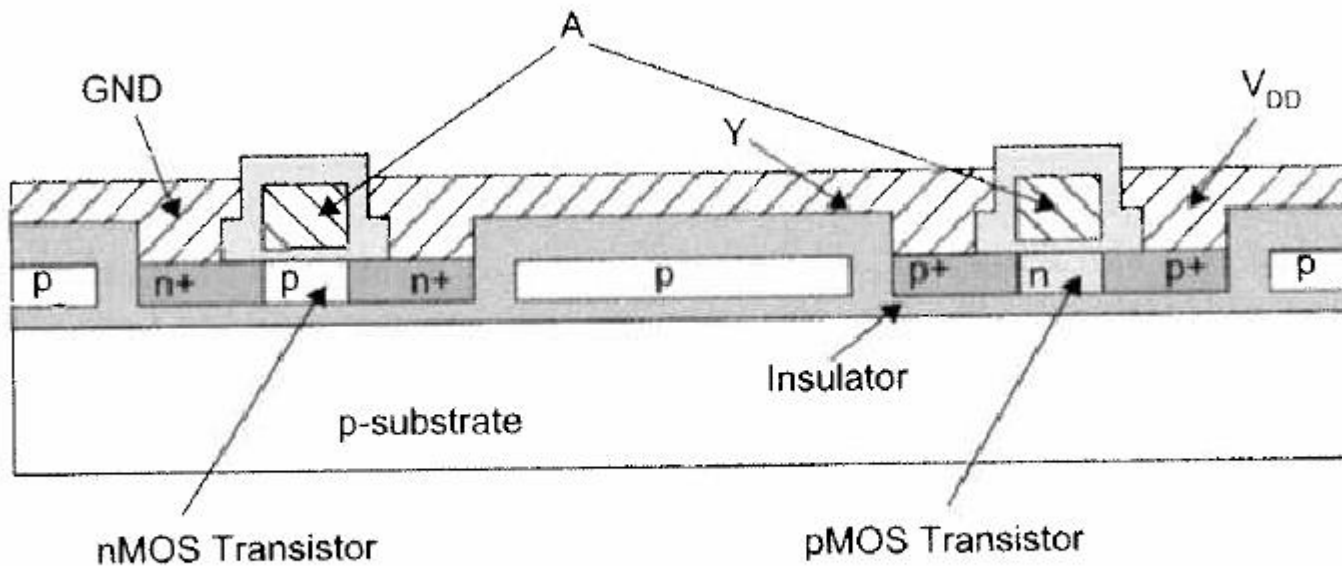
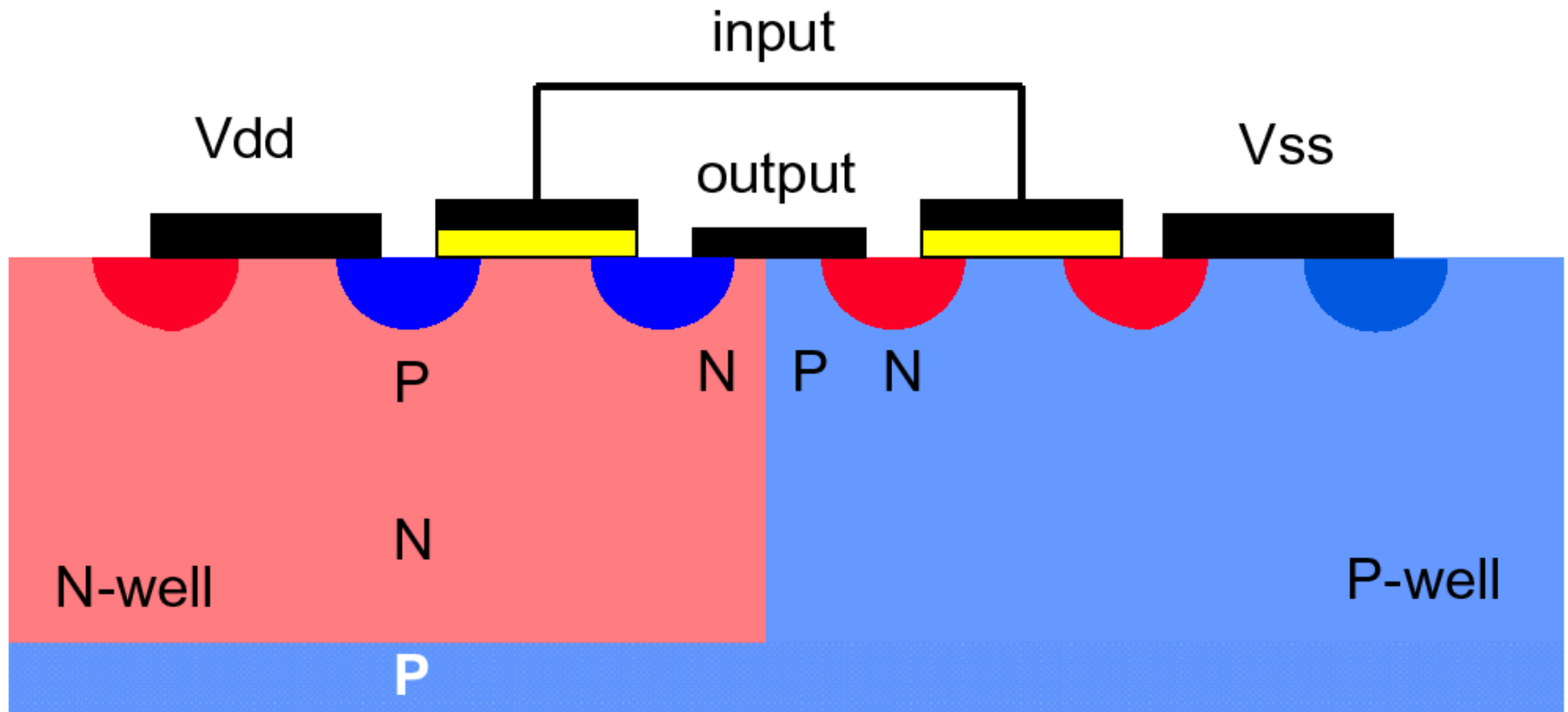


FIG 6.69 SOI inverter cross-sections

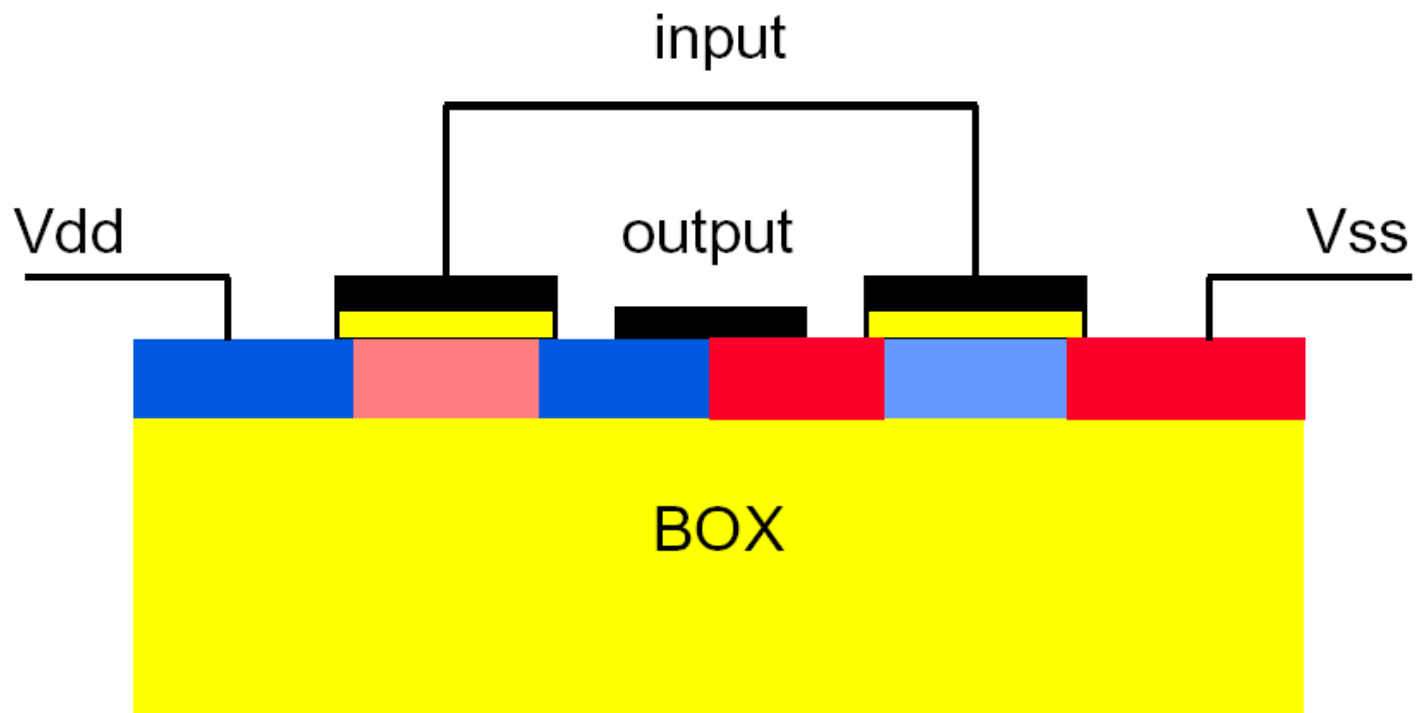
Source: Weste/Harris

Latchup in Bulk CMOS



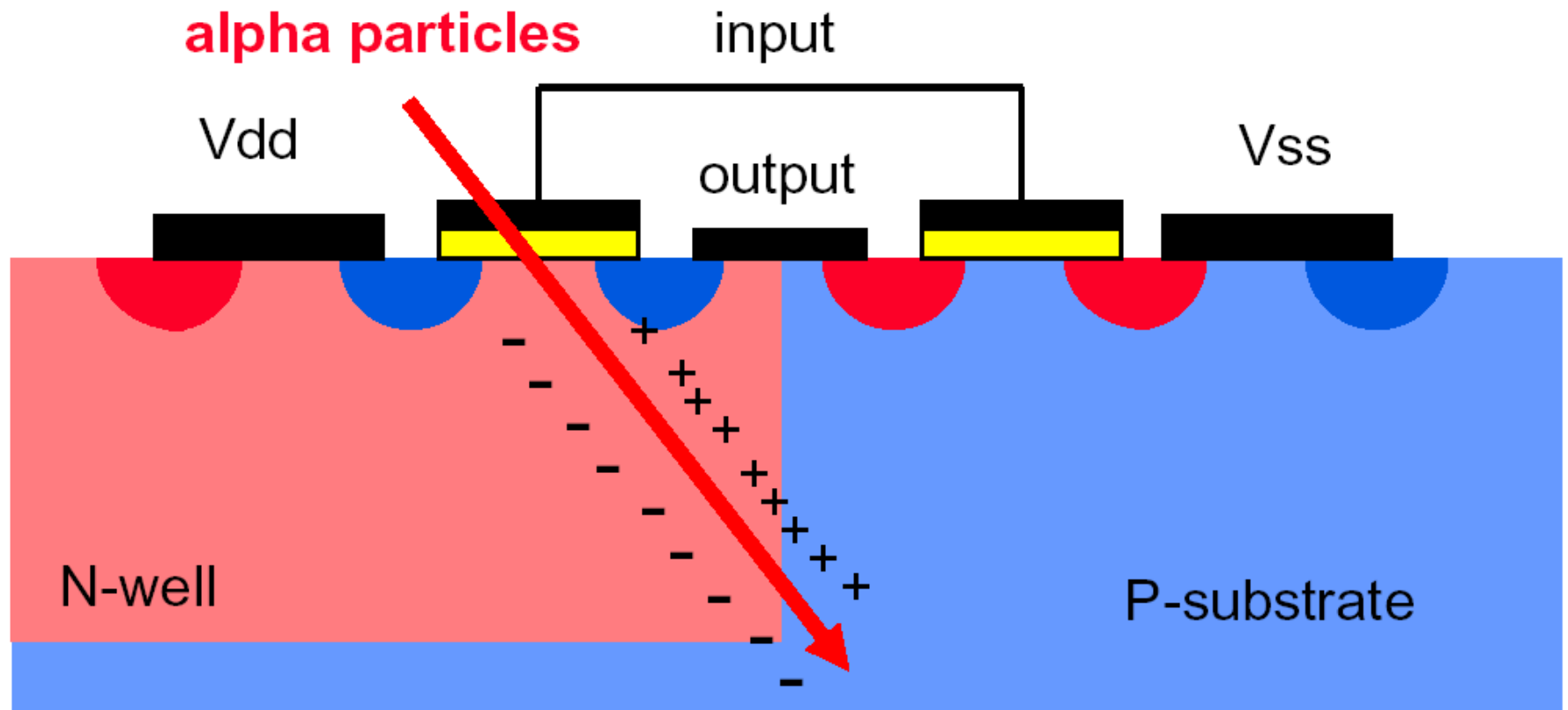
Parasitic bipolar devices → “latchup”

benefits of SOI



No parasitic bipolar devices → no latchup

soft errors in bulk CMOS

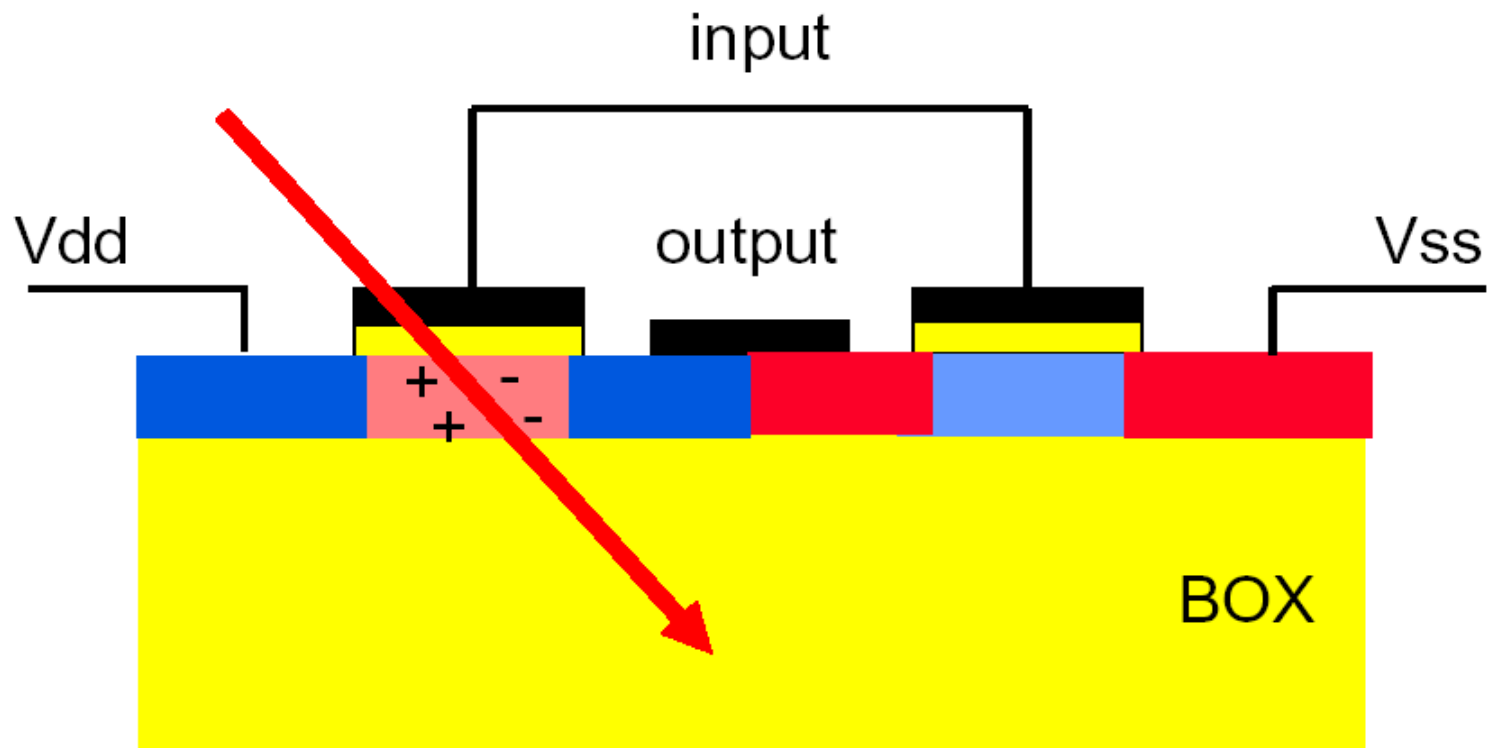


Alpha particles



“soft” errors

soft errors in SOI



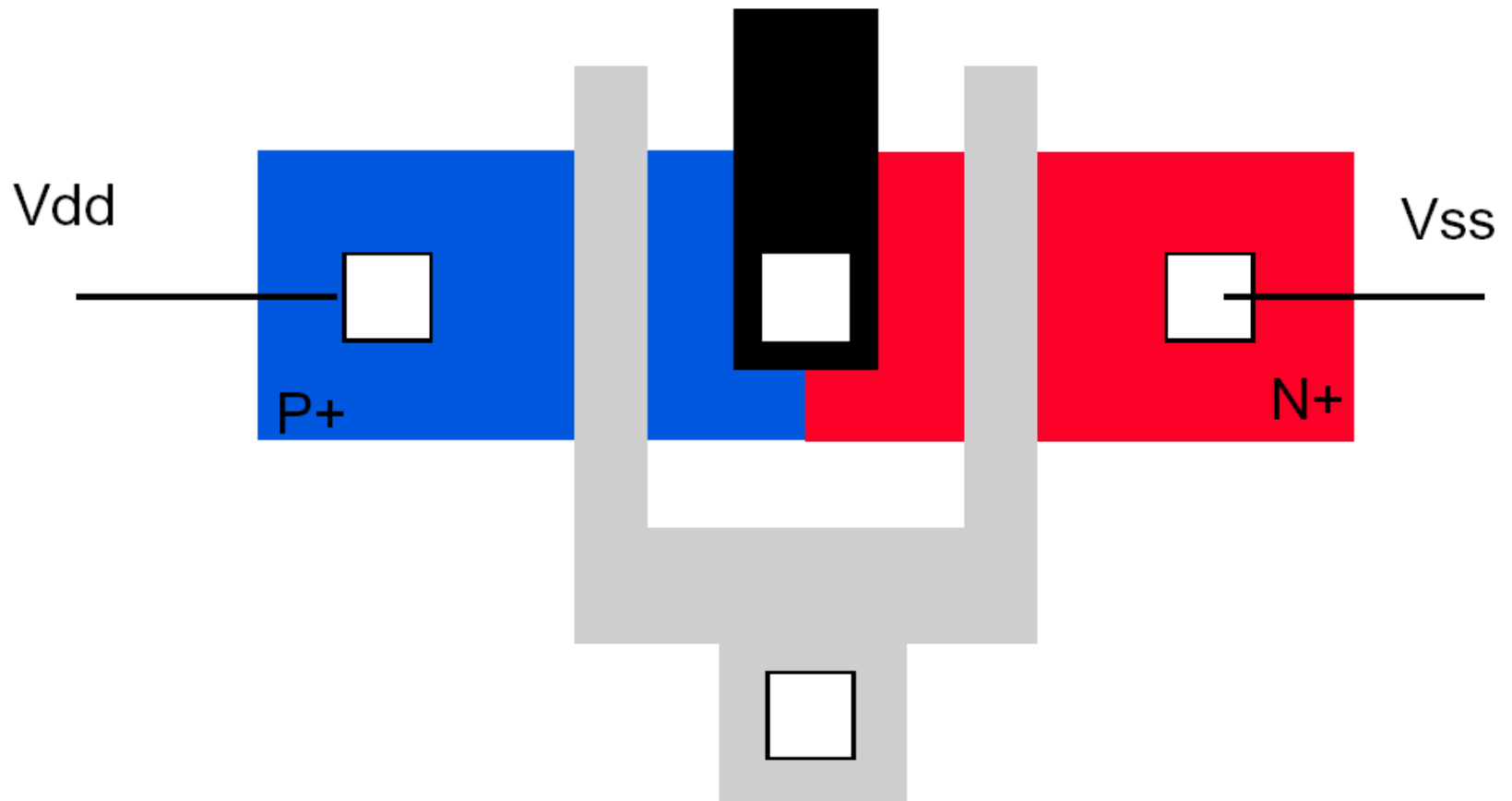
Not as much substrate to generate charge in!

Low soft error rate

layout for bulk CMOS



layout for SOI



Simpler isolation → simpler process → smaller layout

benefits of SOI

- Simple IC processing (isolation)
- Higher density
- Reduced S/D junction capacitance (speed/power)
- Low soft-error rate
- No latch-up
- No (normal) body effect

SOI -> Multigate FET

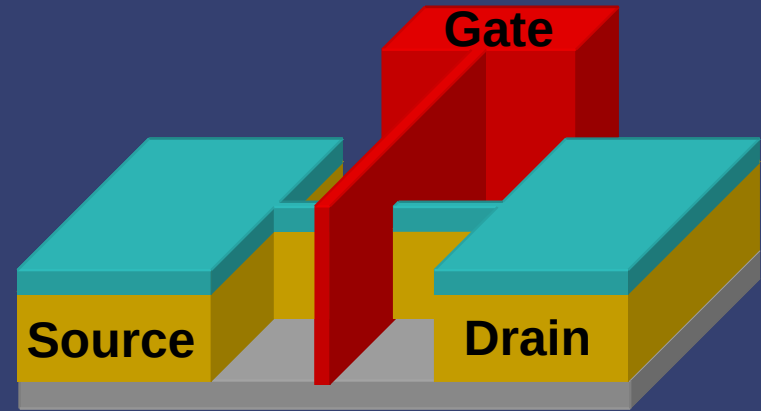
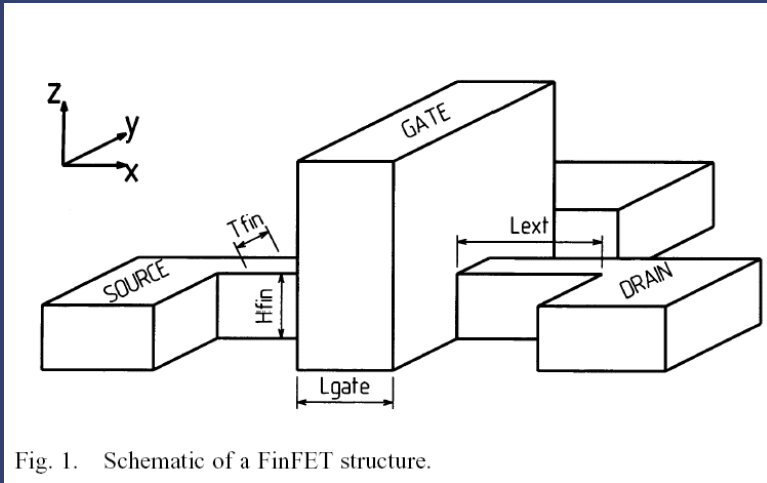
Device Design (Electrostatics)

Single gate	$\lambda_1 = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}}} t_{si} t_{ox}$
Double gate	$\lambda_2 = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}}} t_{si} t_{ox}$
Quadruple gate (square section)	$\lambda_4 \cong \sqrt{\frac{\epsilon_{si}}{4\epsilon_{ox}}} t_{si} t_{ox}$
Surrounding gate (circular section)	$\lambda_o = \sqrt{\frac{2\epsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \epsilon_{ox} t_{si}^2}{16 \epsilon_{ox}}}$

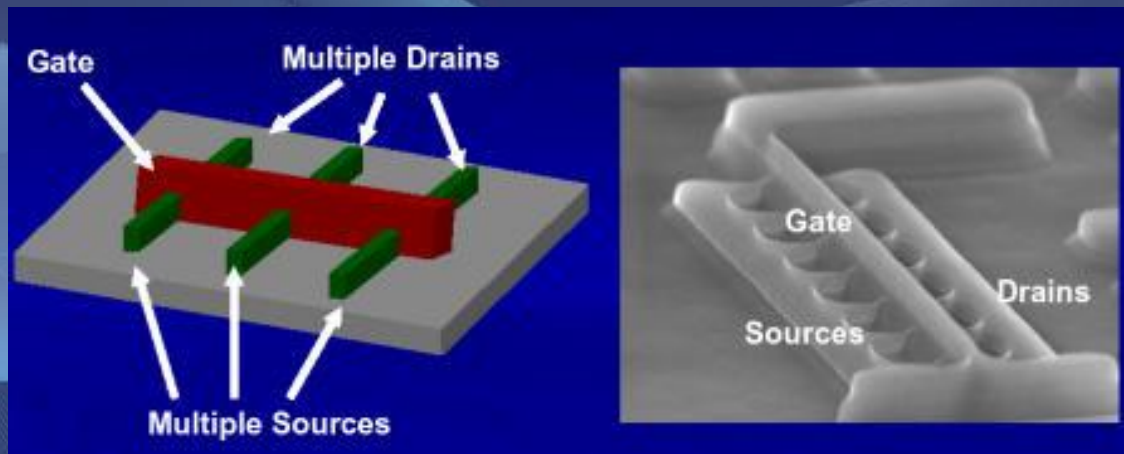
λ : natural length-- an indicator of device scaling ability.

$L_{eff} > 2.5\lambda$ is the bottom line to sustain an acceptable electrostatics.

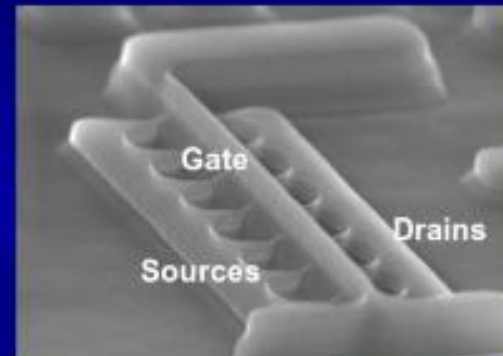
What does FinFet look like?



3D view of FinFET

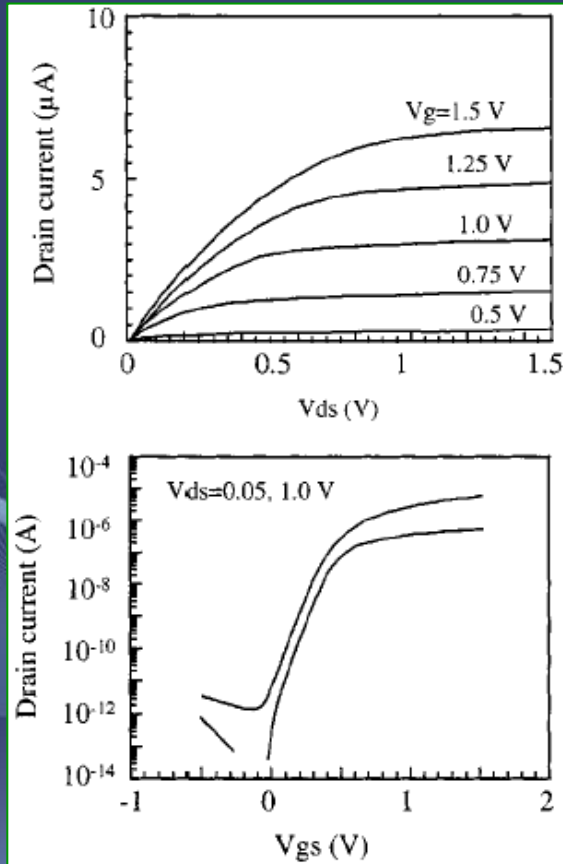


3D view of multi-fin
FinFET



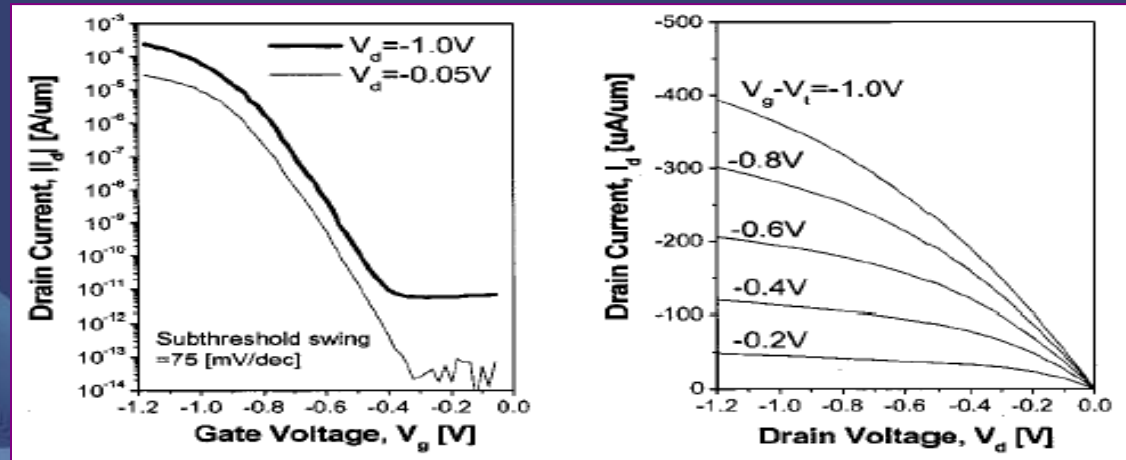
UC Berkeley Results – FinFET/ Double Gate (2000-04)

NMOS



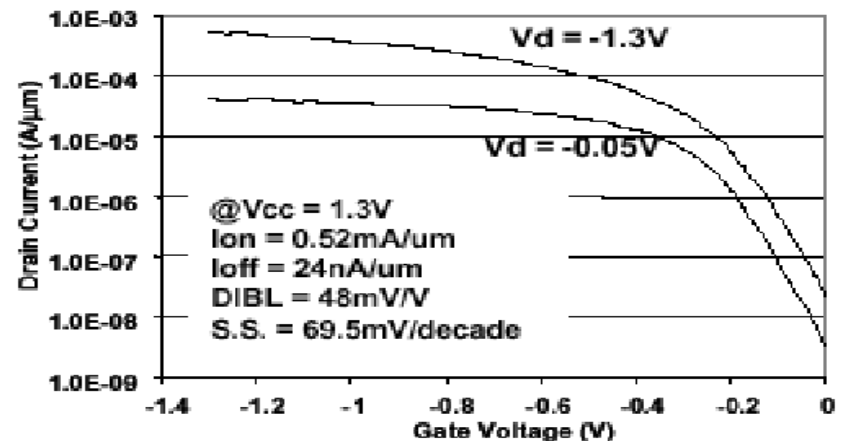
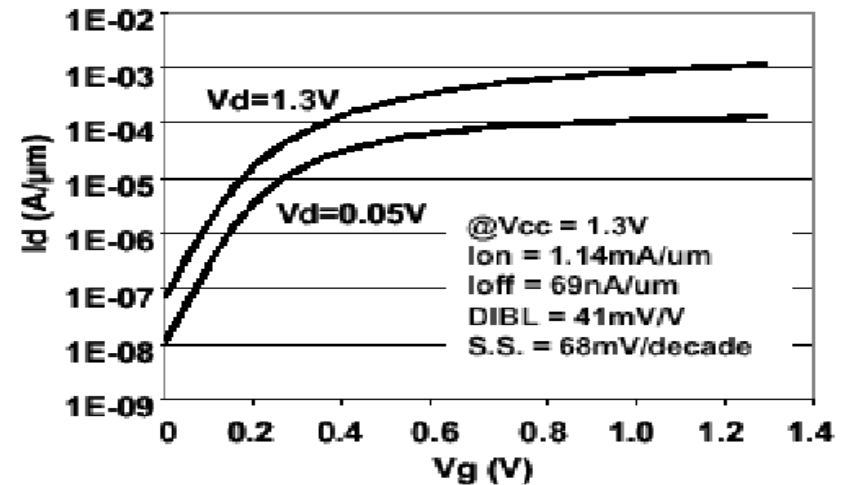
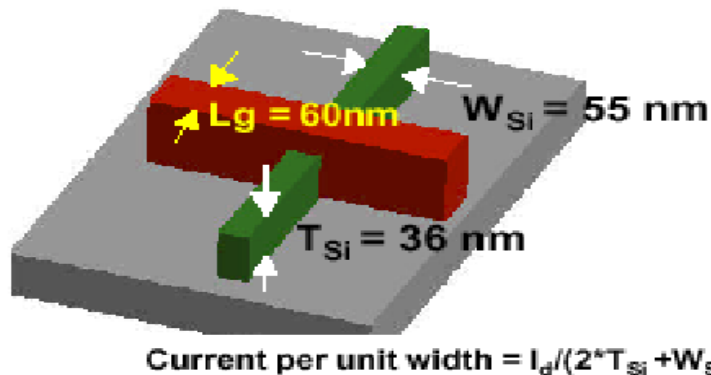
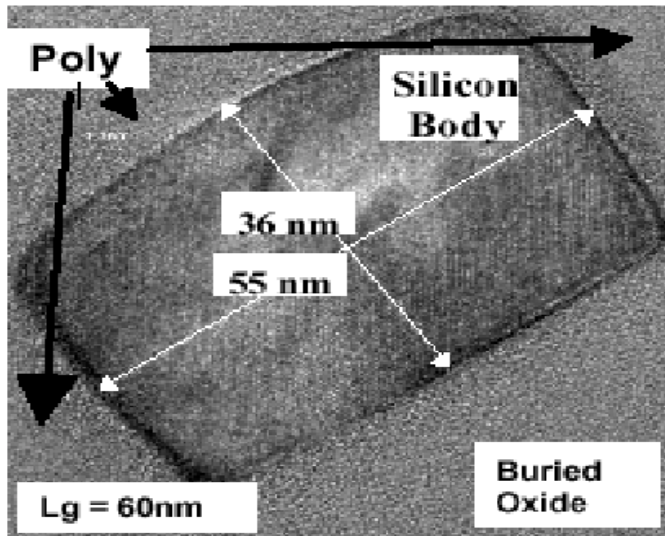
Gate Length = 30nm, Fin Width = 20nm

PMOS



Gate Length = 30nm, Oxide thickness = 2.1nm

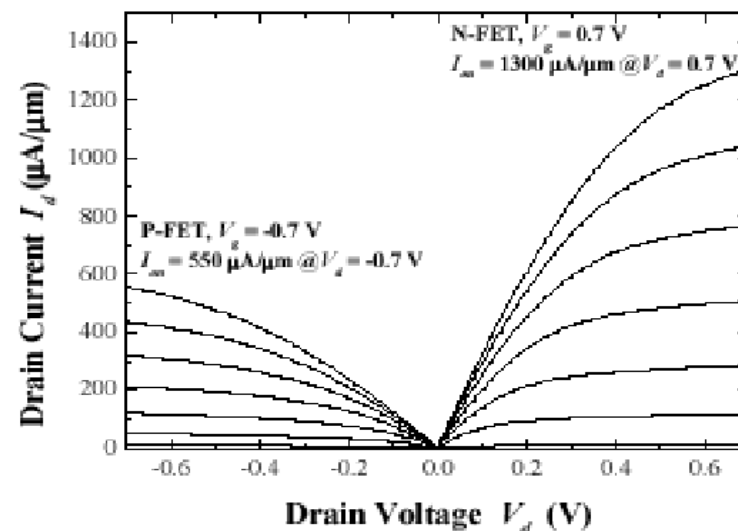
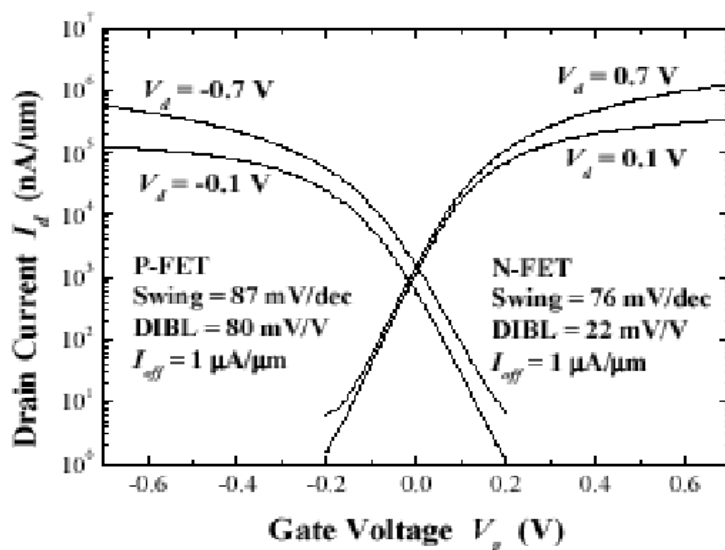
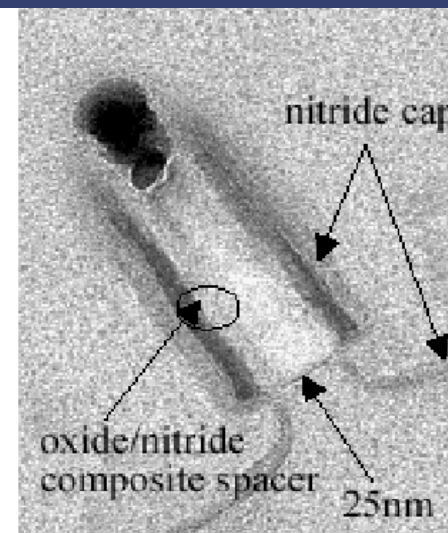
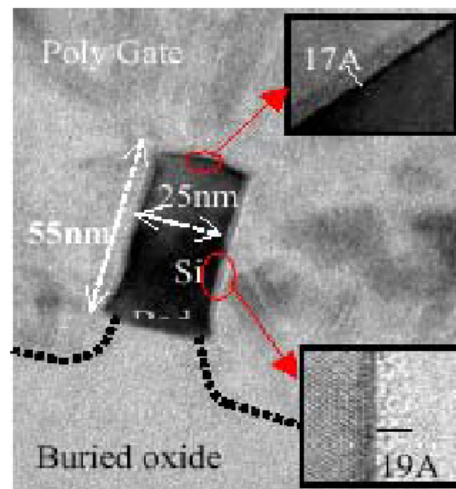
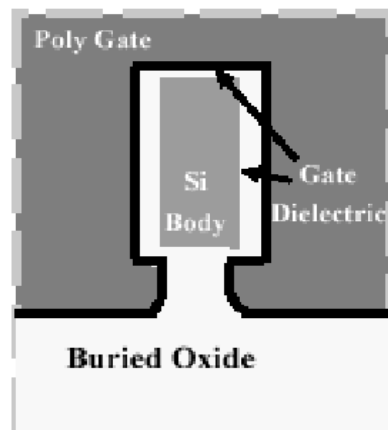
INTEL's TriGate FinFET (SSDM 2002)



Highest ever performance reported for NMOS and PMOS devices on a single substrate !!

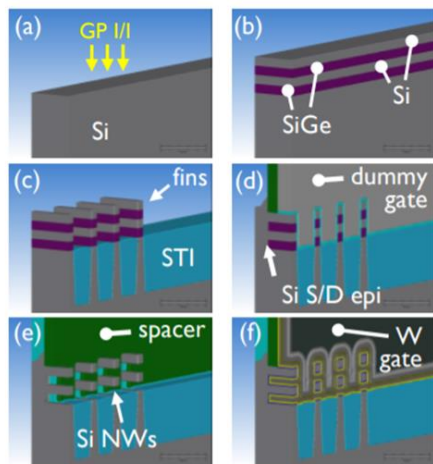
TSMC's Ω -gate FINFET (SSDM-2002)

TSMC's Ω -gate (IEDM'02)

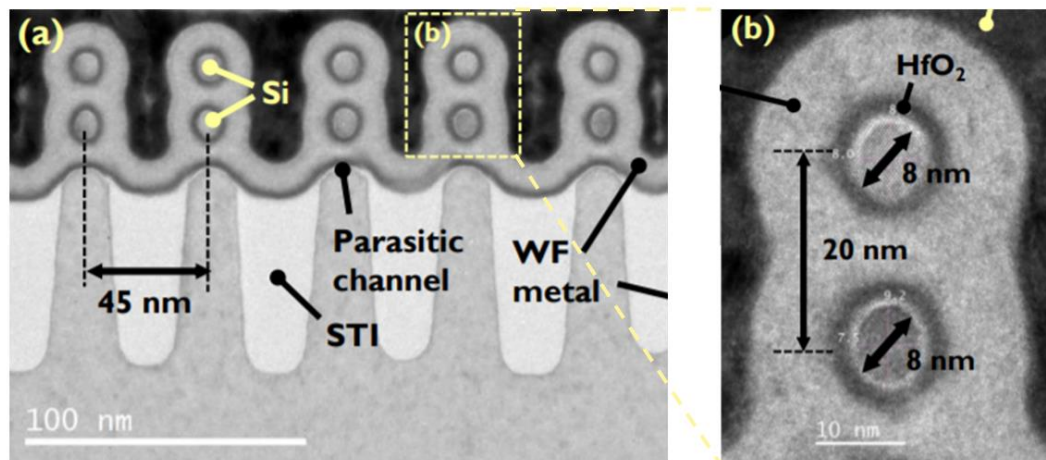


IMEC's Stacked Si Nanowire (2016 VLSI Symp.)

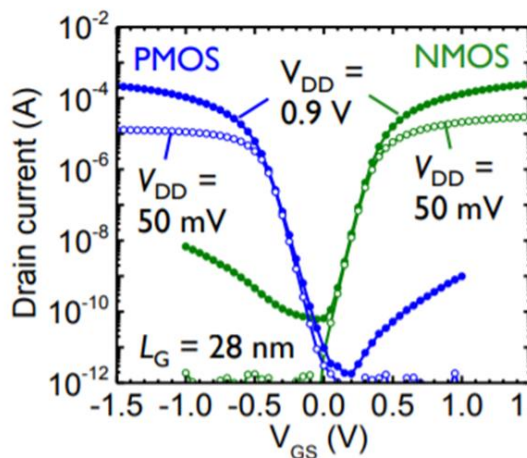
Process Flow



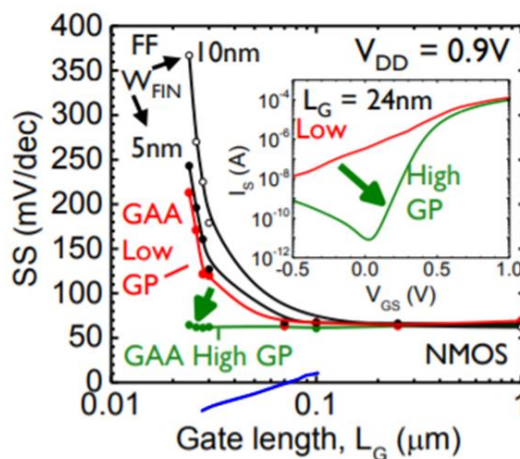
TEM of Vertically Stacked Nanowires



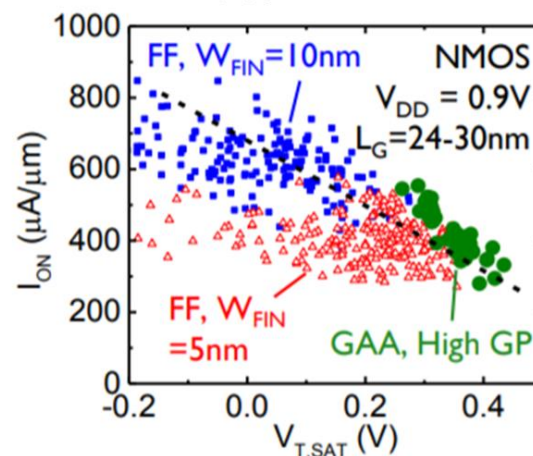
$I_{DS} - V_{GS}$



$SS_{min} - L_G$ scaling

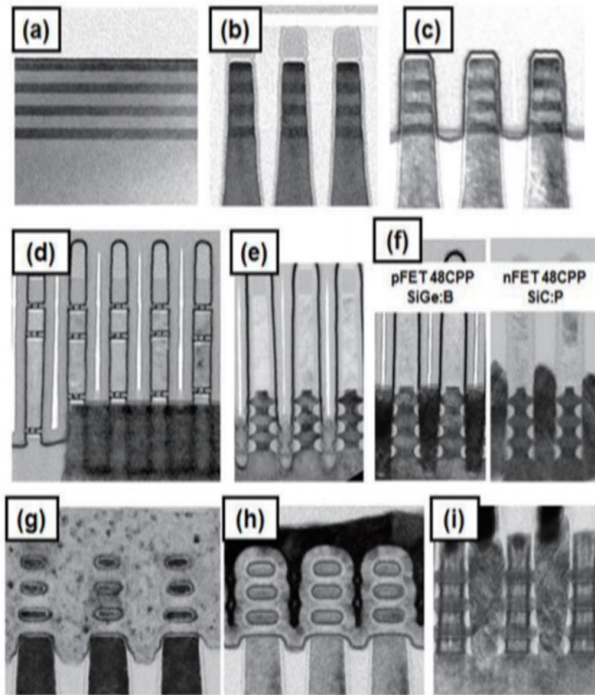


Performance w.r.t FinFET

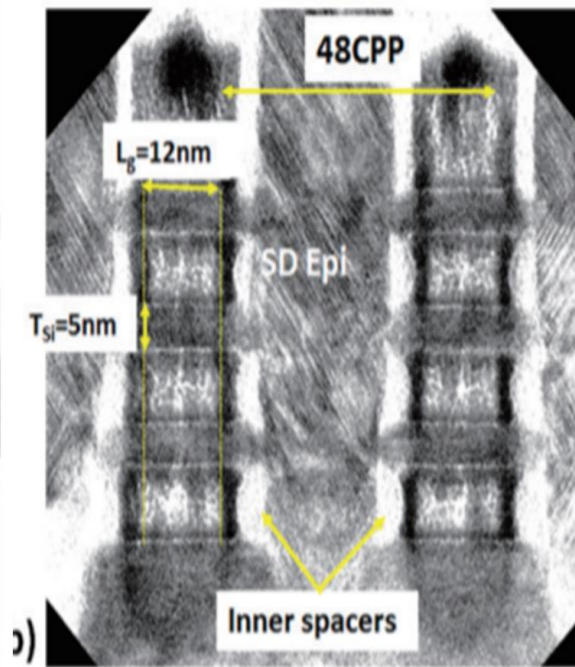


IBM's Nanosheet (2017 VLSI Symp.)

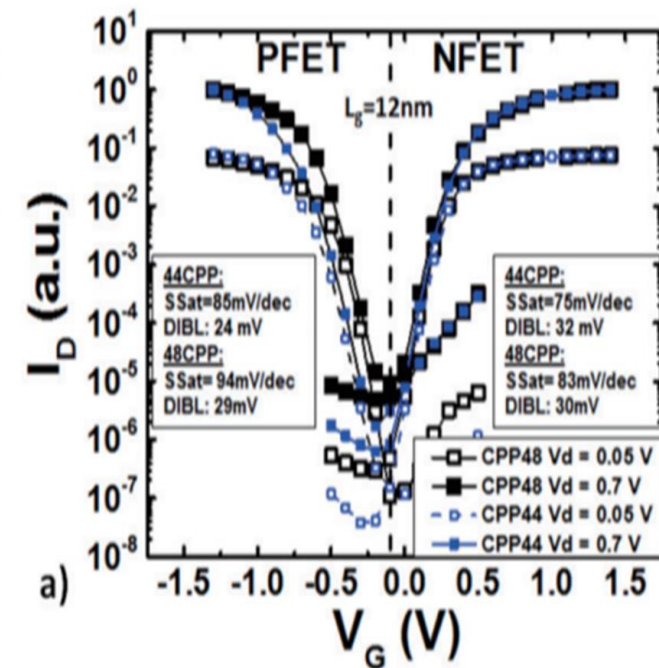
Process Flow



3 Stacked Nanosheets



$I_{DS} - V_{GS}$ Characteristics



Low Power Switch ?