University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #1

Due Date: Feb 23rd, 5 pm, via GradeScope

Problem 1 – CMOS Design (15 pts)

Write a "300 word" essay summarizing your understanding of Moore's Law, major challenges for keeping the law alive, and the role of Heterogeneous Integration for beyond-Moore integration.

Problem 2 – CMOS Design (20 pts) (2+2+2+2+6+6)

Draw the transistor level schematic of a 4-1 Multiplexer with:

a) transmission gate

b) pass transistor logic

c) pass transistor with restoring logic

d) static CMOS

e) Implement all above logic families in Hspice, use 90 nm (available on course website) technology. Compare power, delay and power-delay product of different multiplexers at room temperature.

f) Change temperature to 100°C and repeat part (e).

Problem 3 - MOSFET Physics and Short Channel Effects (15 pts) (5+5+5)

Consider a n-type MOSFET with a p-substrate. As we keep reducing the channel length of the transistor, we run into several short channel effects where the control of the gate on the channel potential is reduced, and the drain starts affecting the channel potential. This leads to degradation in the transistor performance metrics and is very critical as technology nodes keep going down. Here we are going to discuss several of the short channel effects in a conventional MOSFET and their solutions.

a) How can high-K dielectrics and strain engineering help us overcome the short channel effects? Discuss the straining of the channel material of modern FinFETs.

b) What is the main difference between Schottky contact and Ohmic contact? How can you change a Schottky contact to an Ohmic one?

c) What is the purpose of silicided and raised source/drain contacts in advanced MOSFETs?

Problem 4 - MOSFET Electrostatics (20 pts) (4+4+4+4+4)

Read the paper on MOSFET scaling (R. H. Yan et al., "Scaling the Si MOSFET: From Bulk to SOI to Bulk," IEEE Transactions on Electron Devices, vol. 39, no. 7, pp. 499-502, 1992.). Derive the expressions for the Natural Length (λ) for the following devices:

a) Planar Bulk MOSFETs (with and without high-k dielectric)

b) Ultra-thin Body (UTB) SOI MOSFETs (partially depleted and fully depleted)

c) Double-gate FETs: (FinFET) and Tri-gate FET

d) Gate-all-around nanosheet transistors (or a nanowire FET)

e) MOSFETs with 2D-channel materials.

What do you think are the limitations of such analyses based solely on the surface potential?

Problem 5 Leakage in Transistors (20 pts) (5+5+5+5)

(a) Discuss the importance of low leakage current in MOSFETs. Discuss in brief, the origin of the following leakage currents in a MOSFET:

i. Subthreshold Current
ii. Punchthrough
iii. Gate Oxide Leakage
iv. PN Junction Leakage Current
v. Hot Carrier Injection

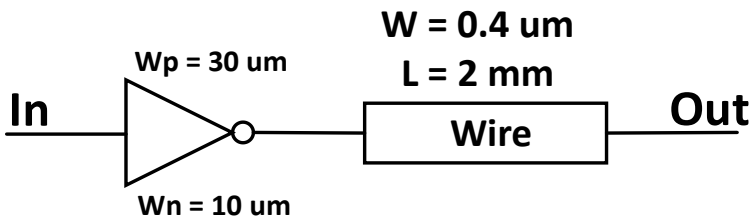
(b) Derive the expression for the Subthreshold Swing (SS) of a conventional MOSFET. How can we get to a perfect SS of 60 mV/dec?

(c) Among the most promising solutions proposed to combat the low SS of a MOSFET, Tunneling Field Effect Transistors (TFETs) have garnered the most attention. Explain with the help of band-diagrams and by using simple equations (if necessary) how can TFETs yield sub-60 SS of drain current? You can explain either a n- or a p-TFET.

(d) What factors determine the minimum and average SS of TFETs?

Problem 6 – Interconnect and Repeater Insertion (10 pts) (5+5)

The following figure shows an inverter driving a piece of wire. Assume that all transistors are minimum channel length (L = 0.25 um) and have the following characteristics: gate capacitance C_G = 2 fF/um, drain capacitance C_D = 1 fF/um, and channel resistance $R_{sqn} = R_{sqp}/2$ = 15 kΩ/Square. For the wires, assume that: parallel plate capacitance C_{wpp} = 0.1 fF/um^2, fringing capacitance $C_{wfringe}$ = 0.05 fF/um per edge, and wire resistance R_w = 0.2 Ω/Square.



a) Draw the RC model you would use to calculate the delay of the circuit shown above from **In** rising to **Out** falling. Replace the wire with a single section π *model* and calculate the values of the resistance and capacitance in your model.

b) What is the Elmore delay from **In** rising to **Out** falling?