University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #2

Due Date: March 8th, 5:00 pm via GradeScope

Question 1 – Minimum V_{DD} for Different Logic Styles (20 pts)

The minimum supply voltage (V_{DD}) for a static CMOS inverter gate was discussed and derived in class. Using similar approach, derive the minimum VDD for the following inverter logic styles:

a) Pseudo-NMOS
b) Resistive load inverter
c) Pass-transistor logic
d) Dynamic gate.

Discuss all possible cases and state any assumptions. Partial credit will be given based on your efforts.

Note: You may supplement your analytical solutions with SPICE simulations to provide additional support.

Question 2 – RC Delay (20)

Consider a uniform interconnect of length L, resistance per unit length r and capacitance per unit length c that is buffered by N identical repeaters (inverters). Assume that for a minimum sized repeater, the input capacitance is c_0, the output parasitic capacitance is C_s, and output resistance is r_s. The interconnect drives a load C_L (input capacitance of each repeater). If the length of the interconnect segment between adjacent repeaters is l (= L/N) and the repeater size is s, then:

(A) Explain why is it necessary that the repeaters are of identical size. Reconcile this with the fact that we have spent long hours understanding why and how gates have to be sized to minimize delay. (4')

(B) Find the delay (τ) of each repeater-interconnect-repeater block. Define the delay (τ) as the time difference between the input of the first repeater and the input of the second repeater. (4')

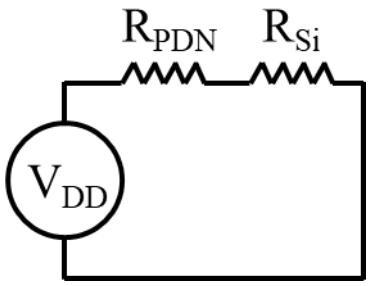
(C) Find an optimum value for s (s_{opt}) that makes total interconnect delay minimum. (4')

(D) Find an optimum value for l (l_{opt}) that makes the total interconnect delay minimum. (4')

(E) Find the minimum value of the total interconnect delay τ_{opt}. (4')

Question 3 – IR Drop and Self-Heating (20)

Consider an equivalent circuit of a power-delivery-network (PDN) and the transistors in the active layer of Si to consist of two resistors in series (R_{PDN} and R_{Si}) power by a voltage source V_{DD}.



The maximum power (P_{max}) transferred to the active layer is equal to V_{DD}^2/R_{Si}, when $R_{PDN} = 0$.

1. R_{Si} is given by the equation $R_{Si} = \alpha(2V_{DD}V_{Si} - V_{Si}^2)$. Find out, in terms of P_{max}, how much power (P_{Si}) is transferred to the active layer for an IR (voltage) drop of 0, 5, and 10 % V_{DD} across R_{PDN}. (5 + 5 + 5).

2. The current in the PDN will induce self-heating and thus raising the temperature of the metal lines in the PDN. How will this impact the resistance of the PDN (R_{PDN}) and power transferred to the active layer (R_{Si}). (5)

Question 4 – Three-Dimensional Integration (20 pts)

Read the article to be posted under the Lecture "3D Integrated Circuits", by *Banerjee et al., Proceedings of IEEE, 2001*, and answer the following questions.

1. What are the benefits of 3D integration?

2. Prepare a table summarizing various 3D ICs introduced so far by commercial entities and their timelines. What is the total 3D IC market (in billions of dollars) and what are the projections?

3. What are the current 3D IC fabrication methods? List the various challenges?

4. What are the benefits of monolithic 3D integration? Why are 2D materials beneficial for monolithic 3D integration?

Question 5 – Non-conventional memory technologies (20 pts)

Summarize the scaling challenges for different types of memories, including **SRAM**, **DRAM**, **flash memory**, **3D-NAND**, **memristor**, **Phase Change Memory (PCM)**, **Spin Torque Transfer Magnetic Memory (STT-MRAM)**, **Resistive Memory (RRAM)**, **Conductive-bridging Memory (CBRAM)** and **Ferroelectric RAM (FeRAM)**. Discuss the advantages and disadvantages of these emerging memory technologies in different applications.