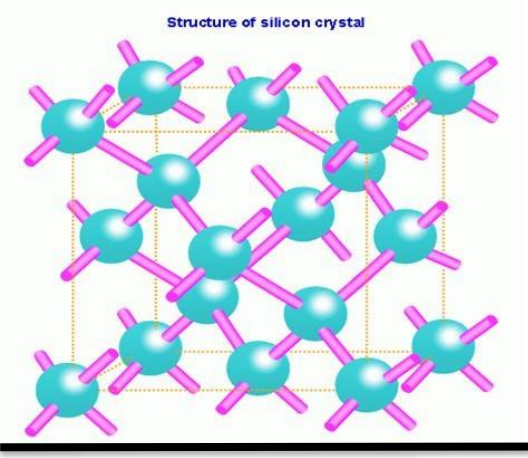

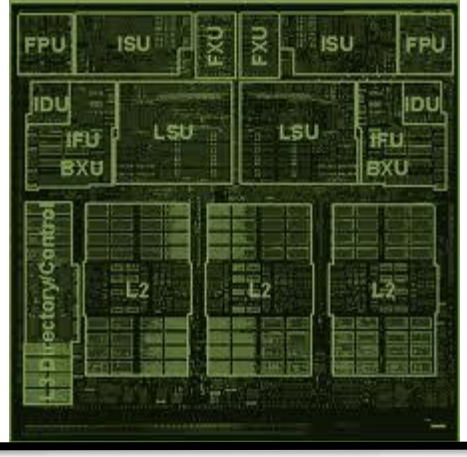

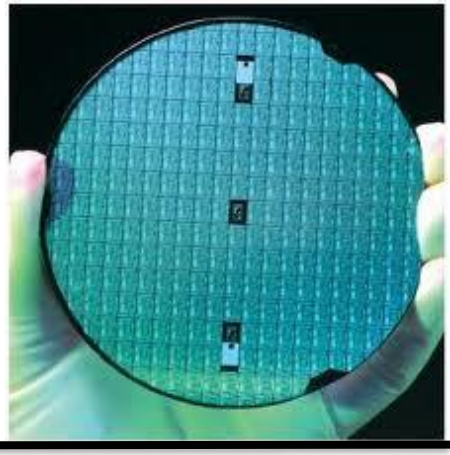

ECE 225
High Speed Digital IC Design
Lecture 2
Discussion of Project Topics

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Electrical and Computer Engineering
University of California, Santa Barbara
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Project Timeline….

- Must work individually…
- Topic/Abstract: Jan 25 (~ 200-300 words)
  - Literature review and identify problem to be addressed within a given topic.
  - Justify your project…
- Final project presentations: toward the end of the quarter (~20 mins per student including QnA)
- Final project report due in March (end of finals week)
  - IEEE Letters style (~5-6 pages)

Project Topic Areas….

- **Emerging Technologies for VLSI and Beyond-Moore Technologies:**
  - emphasis on circuit/system design and optimization

  a. Si-based / CMOS – FinFET, GAA-FET, stacked-Nanowire/Nanosheet- FET

  b. Non-Si / CMOS – such as 2D-FETs, CNT-FETs, etc

  c. Memory technologies - new designs for SRAM/DRAM/Flash with 2D/1D
  - RRAM, MRAM, FRAM, STT-RAM, PCM etc (for NV memory)

  d. Energy-efficient beyond-CMOS devices – TFETs, IMOS, Fe-FET, NEMFET, IMT, etc. - Non-charge (spin) based devices

  e. Monolithic 3D ICs: design architectures for maximizing performance and energy-efficiency, heterogeneous integration (HI), opportunities with new materials and devices, power delivery and thermal management issues

  f. Emerging interconnect technologies: nano-carbons such as graphene, optical, RF interconnects etc.

  g. On-chip inductors/capacitors/antennas (materials, mechanisms, designs…)

  h. Implications for HI and AI (NVIDIA AI chips…)

- **Non-Von Neumann Architectures** - materials, devices, circuits

  a. Neuromorphic computing

  b. In-memory computing

  c. Quantum computing / Cryogenic electronics

Note: The listed topics above are suggestions only. You may choose a topic outside of this list, but prior approval is needed.

66th International Electron Devices Meeting

0.5T0.5R – A "Smart" Transistor with Embedded RRAM

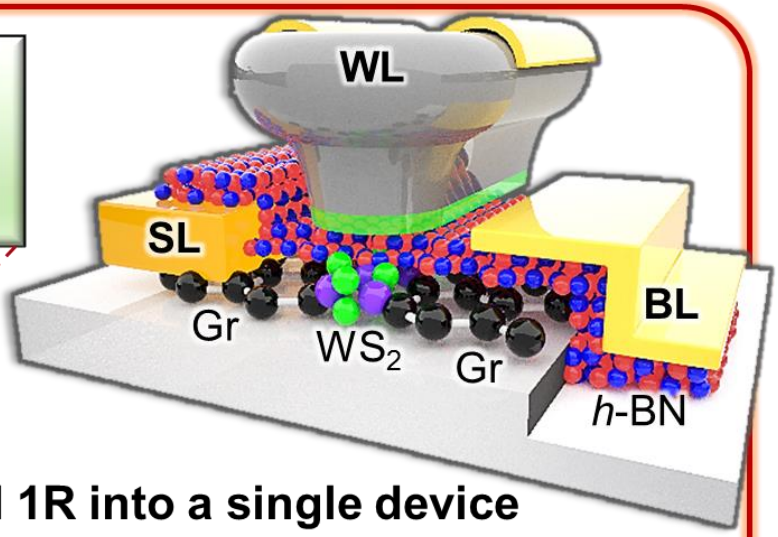
Paper #: 12.3 (Tuesday, Dec 15, 2020)

First ever in RRAM technology history…

Excellent hardware platform for neuromorphic and in-memory computing

0.5T0.5R

Gr-WS_2-Gr HFET + *h*-BN RRAM



Key features:

- **Integrates 1T and 1R into a single device**
- **Uniquely enabled by 2D materials**
- **Reduces device count by half**
- **Enables neuromorphic and in-memory computing**

0.5T0.5R Hybrid Device

- Ultra-compact footprint
- Access latency: < 10 ns
- Programming energy: 0.07 pJ/bit