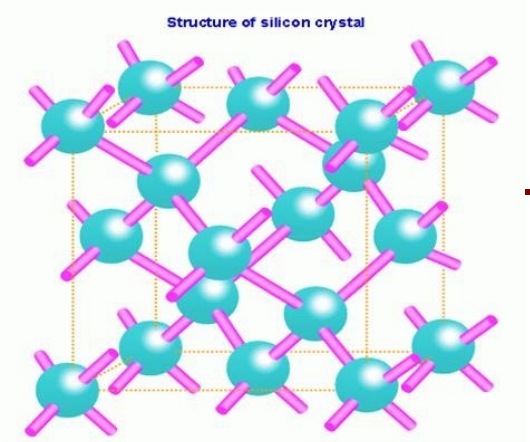

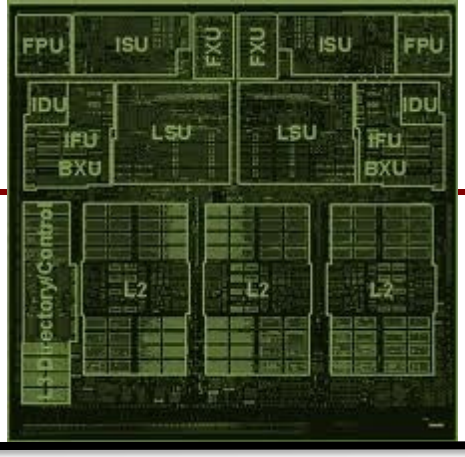

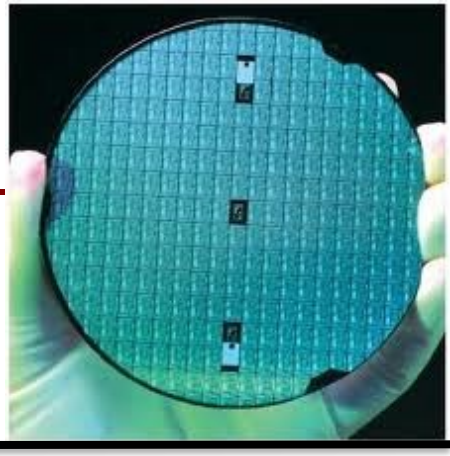

ECE 225

Lecture 13

BEOL Applications of Graphene in Next-Generation ICs

by Kunjesh Agashiwala (PhD Candidate, NRL)

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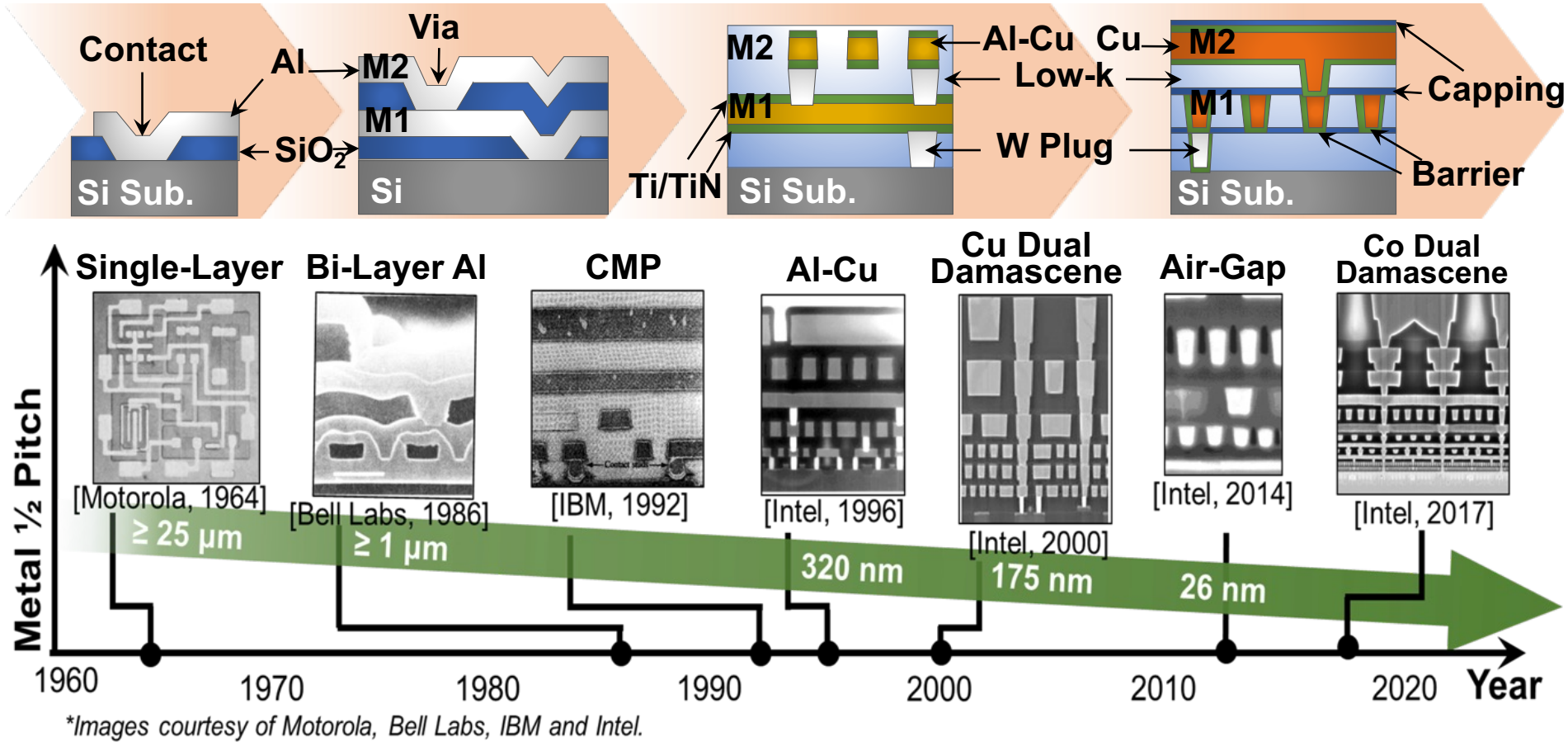
Electrical and Computer Engineering

University of California, Santa Barbara

Outline

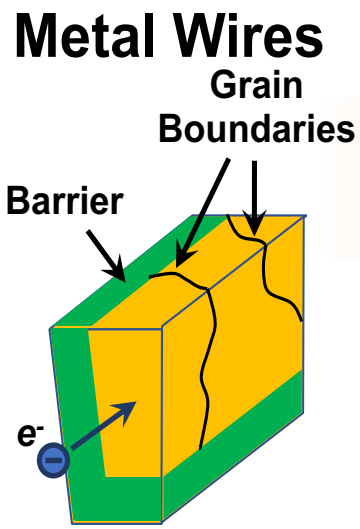
- BEOL Evolution and Scaling
- Graphene based interconnect (wire) technology
- Graphene for capping layer applications
- Graphene based inductors for RF-ICs

BEOL Scaling and Evolution

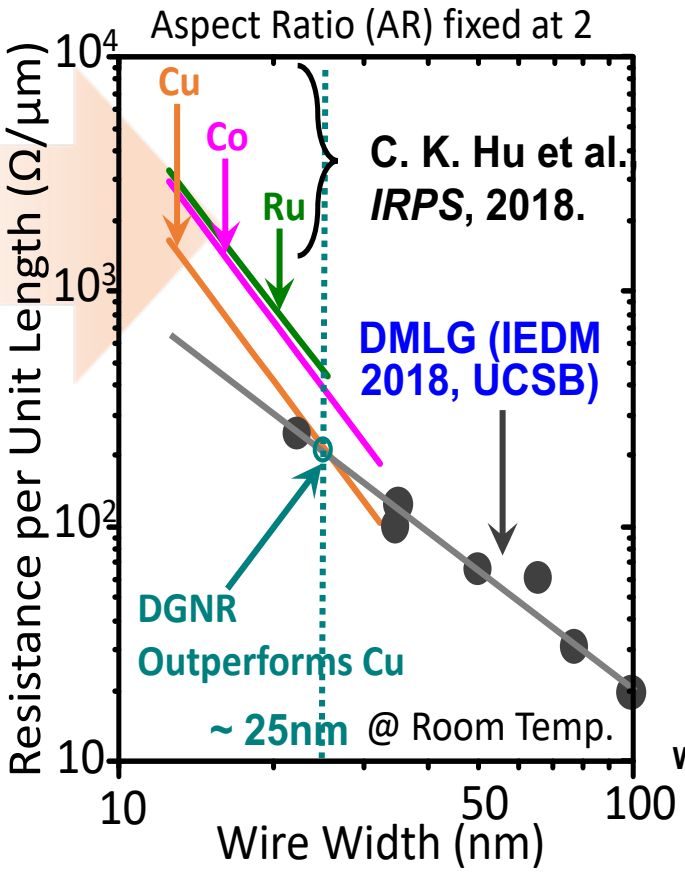


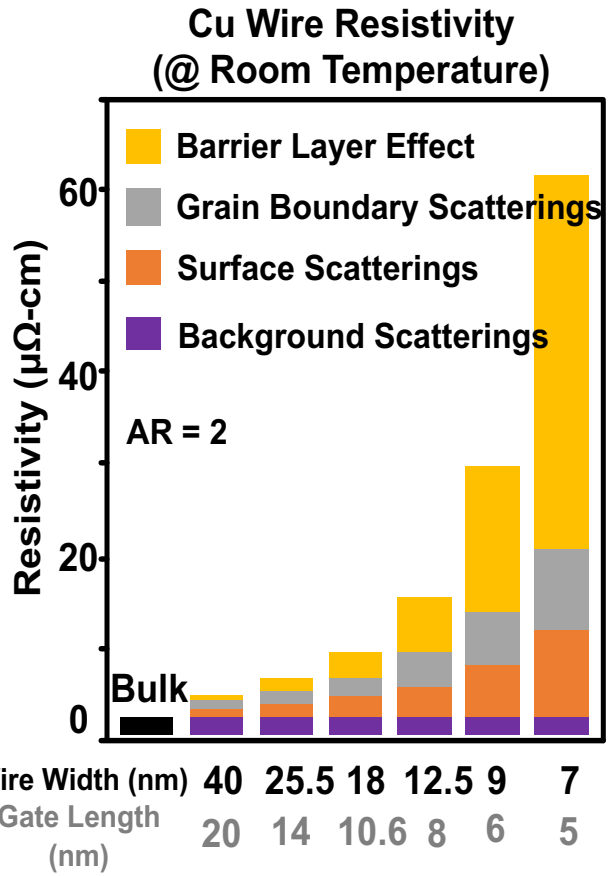
K. Agashiwala, J. Jiang, A. Kumar, C-H Yeh, and K. Banerjee, Chip Scale Review, Nov-Dec 2021.

Interconnect Scaling Challenges



Rapidly Increasing Resistance:
- Barrier layers
- Surface scatterings
- Grain boundary scatterings

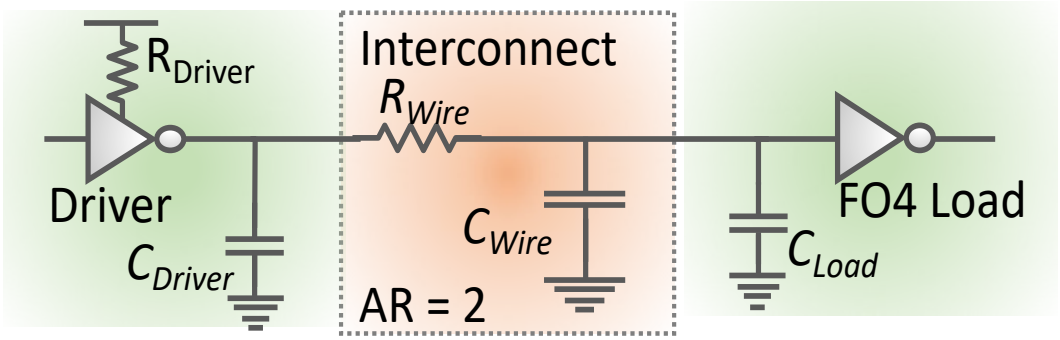




J. Jiang, et al., *IEDM*, 2018.

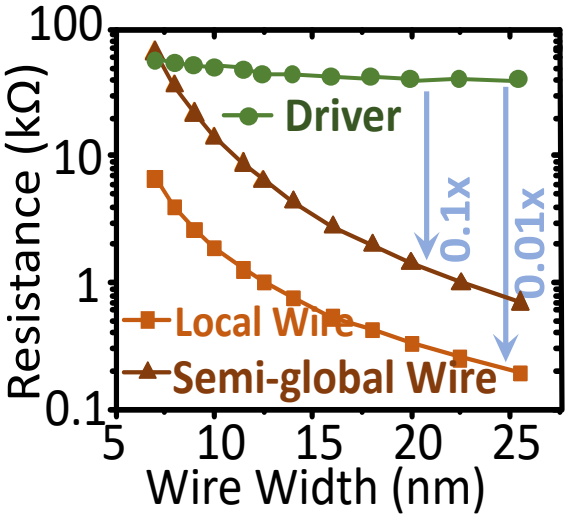
Severe resistance increase for aggressively scaled wires!!

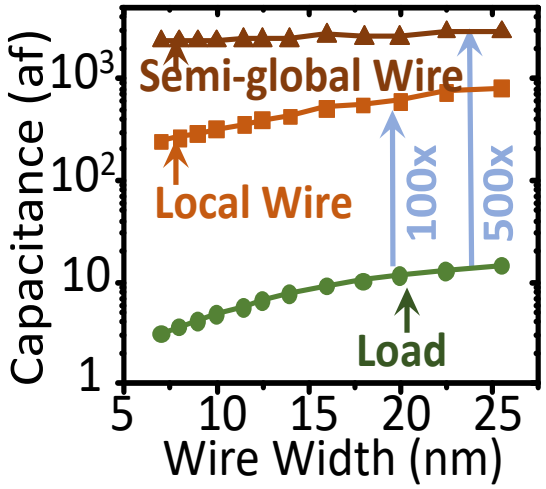
Challenges- Delay and Energy-Efficiency



- Assuming Lumped RC model, the Elmore delay is $R_{Driver}C_{Driver} + \boldsymbol{R_{Driver}C_{Wire}} + R_{Wire}C_{Wire} + R_{Driver}C_{Load} + R_{Wire}C_{Load}$

→ $\boldsymbol{R_{Driver}}$ and $\boldsymbol{C_{Wire}}$ dominates the delay **(Local Interconnects)**





- Switching energy

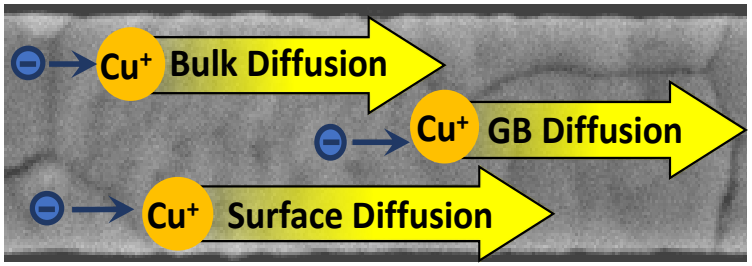
$(C_{Driver} + C_{Load})V_{DD}^2 + \boldsymbol{C_{Wire}V_{DD}^2}$

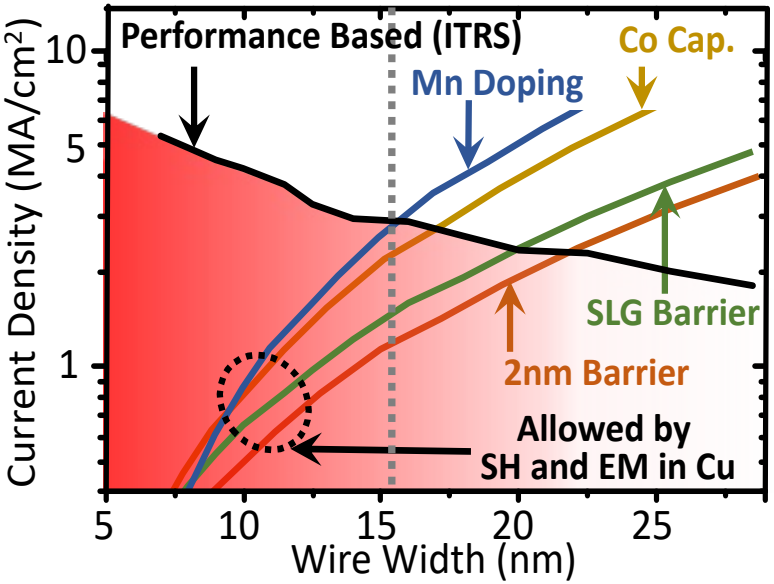
→ $\boldsymbol{C_{Wire}}$ dominates the switching energy

Need to reduce the wire capacitance to control the delay and energy-efficiency!!

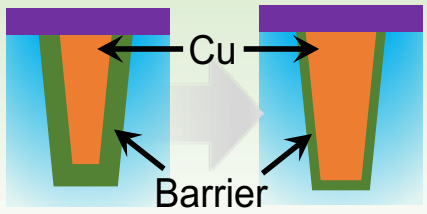
Challenges- Reliability

Cu Migration Under Current Stress



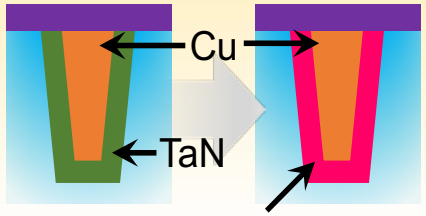


Barrier Scaling



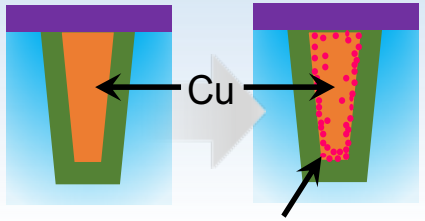
Thinner barriers that stop Cu diffusion → reduce effective *J*

Alternative Barrier/Cap.



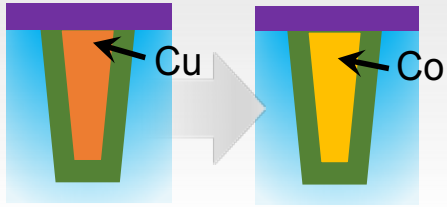
New materials (Co, Mn, etc.) suppress surface diffusion

Cu Alloy (Mn, Al)



Suppress surface/GB diffusion, with R penalty

Alternative Conductor



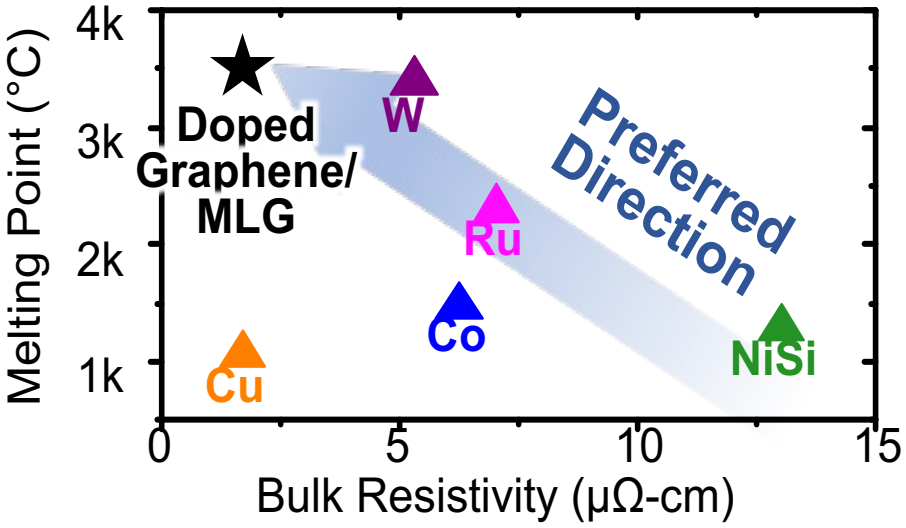
Higher EM resistance, with R penalty

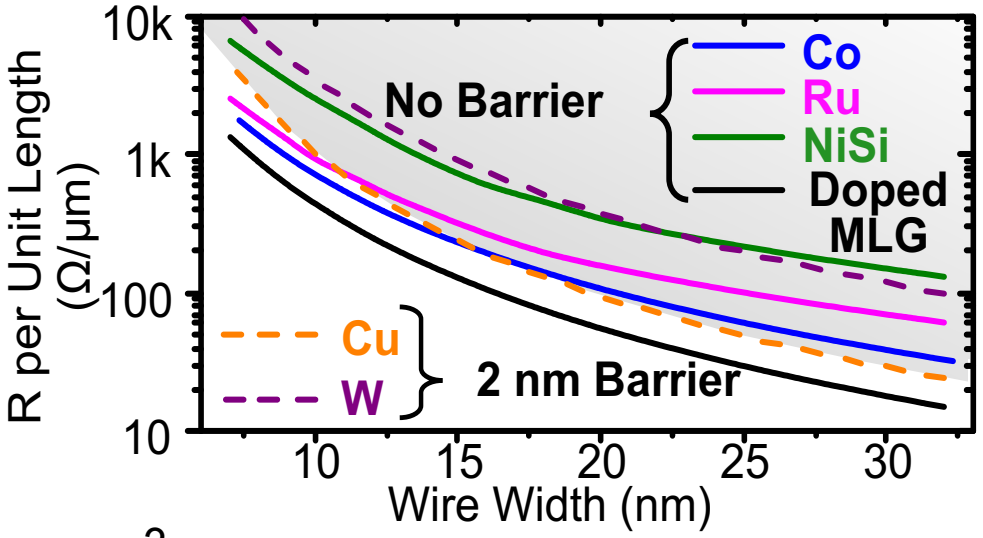
C. K. Hu et al., *MRS*, 2013.
G. Bonilla, *VLSI Symp.*, short course, 2018.
J. Jiang et al., *Nano Letters*, 2017.

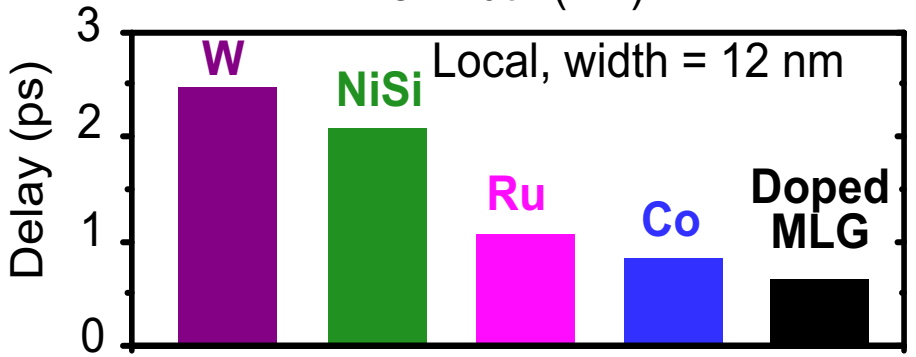
Aggressively scaled wires also need to possess high-current carrying capacity!!

Beyond-Cu Candidates for BEOL

- Potential candidates include metals (Co, Ru, W, etc.), metal alloys, metal silicide (NiSi) and doped multilayer graphene (MLG)





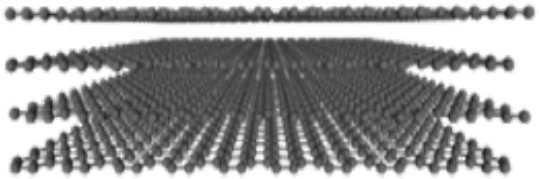


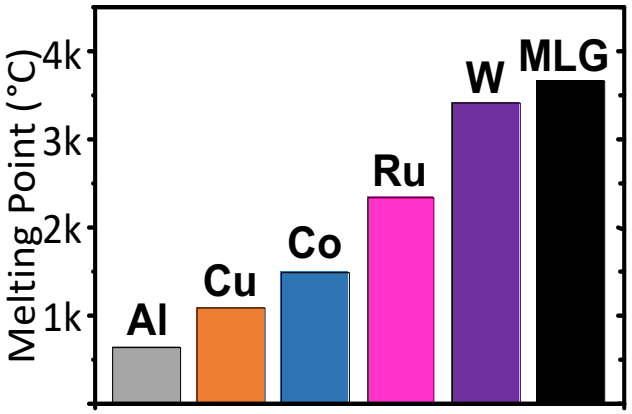
Graphene (or multilayer graphene, MLG) possess lower resistivity, higher current carrying capacity than most conventional metals!!

Why Multilayer Graphene?

Multilayer Graphene (MLG)

- High carrier mobility
- Strong sp^2 bonding
  - High melting point
  - EM resistance
- High in-plane electrical and thermal conductivity
- Lower contact resistance than 1L-graphene

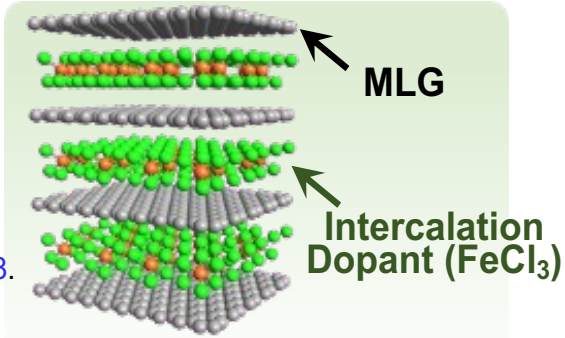




H. Li, et al., *TED*, vol.56, no.9, 2009 (**UCSB**)

Doped Multilayer Graphene (DMLG)

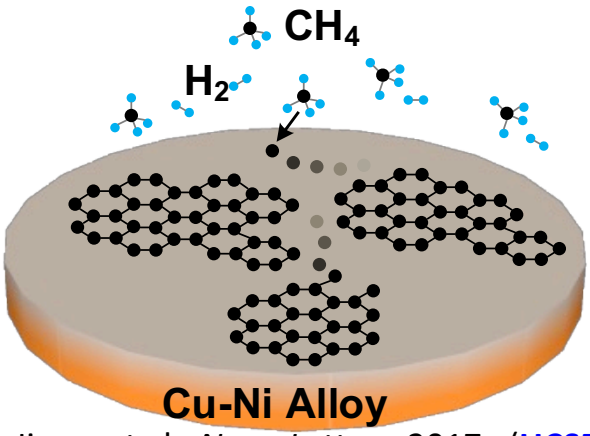
- To compensate for the increase in wire resistivity at sub-50 nm dimensions
- Doping restores the linear band-structure of graphene
  J. Kang et al., *Nature Electronics*, 2018.
- Increases the carrier conc. by charge transfer effect



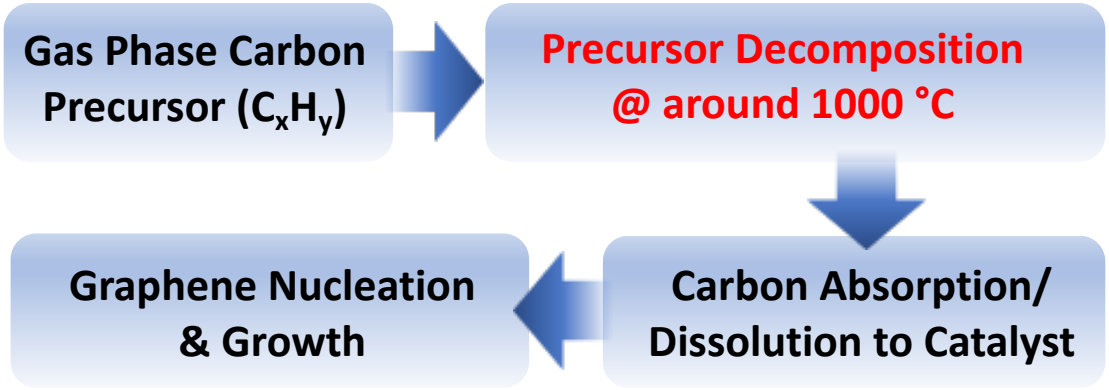
J. Jiang et al., *IEDM*, 2018.

Property	Cu	MLG
Max. current density (MA/cm^2)	10^6	$> 10^8$
In-plane thermal conductivity (W/mK)	385 (bulk)	3000-5000

Conventional MLG Growth by CVD



J. Jiang, et al., *Nano Letters*, 2017. (**UCSB**)

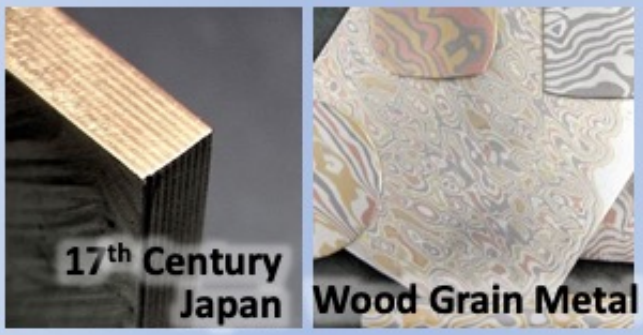


- High-temperature decomposition of gas-phase precursor for carbon supply
- Additional transfer of CVD MLG to desired substrate
- Attempts on low-temperature (< 500 °C) / transfer-free synthesis by CVD produce discontinuous / low-quality MLG
  - Plasma Enhanced CVD @ 500 °C (D. Wei, et al., *ACS Nano*, 2015)
  - Remote Catalyzation @ > 850 °C (P. Y. Teng, et al., *Nano Letters*, 2012)

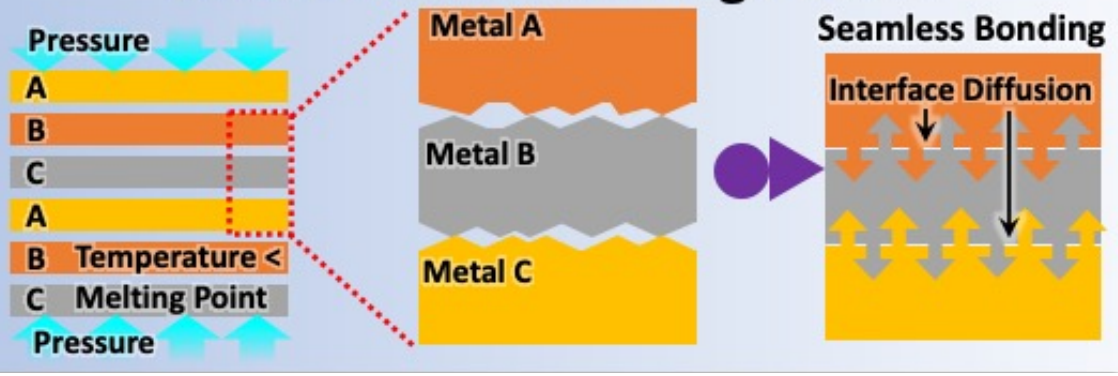
Need temperatures < 500 ^{0}C for the approach to be compatible with BEOL!!

Another Unique Approach to Grow MLG

Mokumegane (木目金)



Solid Diffusion Bonding Process



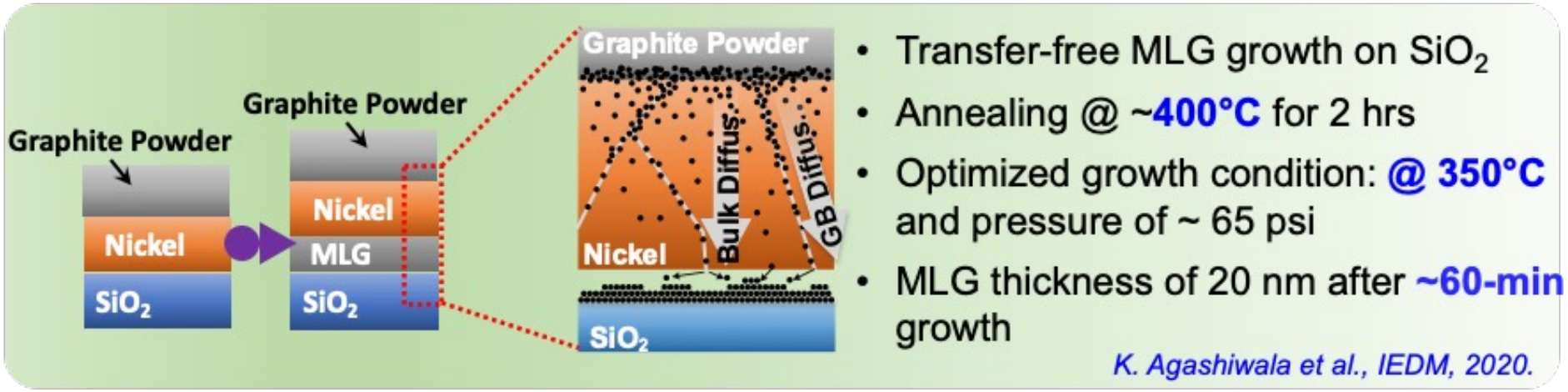
Graphene @ UCSB

- Graphite powder + nickel catalyst
- Optimized condition: **@ 350 °C** and pressure of 65 psi
- Transfer-free MLG growth on SiO_2
- MLG thickness of 20 nm after 30-min growth
- Controllable MLG thickness & quality

J. Jiang et al., *IEDM*, 2018. K. Agashiwala et al., *IEDM*, 2020.

CMOS-compatible pressure assisted MLG growth!!

CMOS-Compatible Pressure Assisted MLG

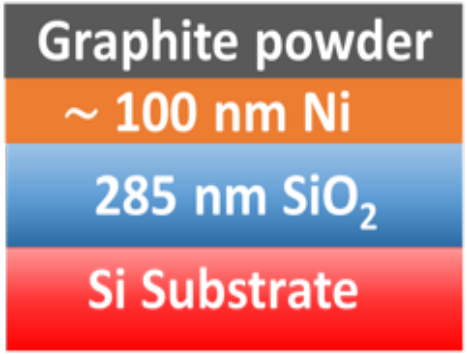


- Transfer-free MLG growth on SiO_2
- Annealing @ ~**400°C** for 2 hrs
- Optimized growth condition: **@ 350°C** and pressure of ~ 65 psi
- MLG thickness of 20 nm after **~60-min** growth

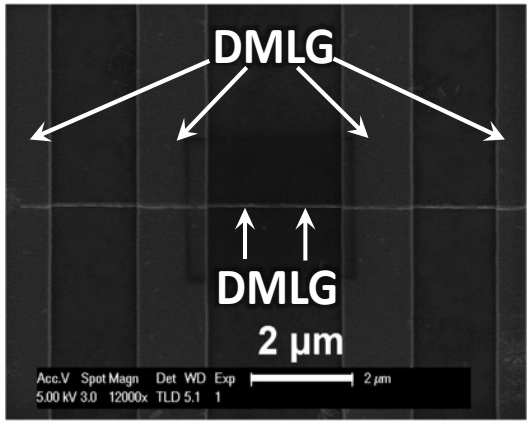
K. Agashiwala et al., IEDM, 2020.

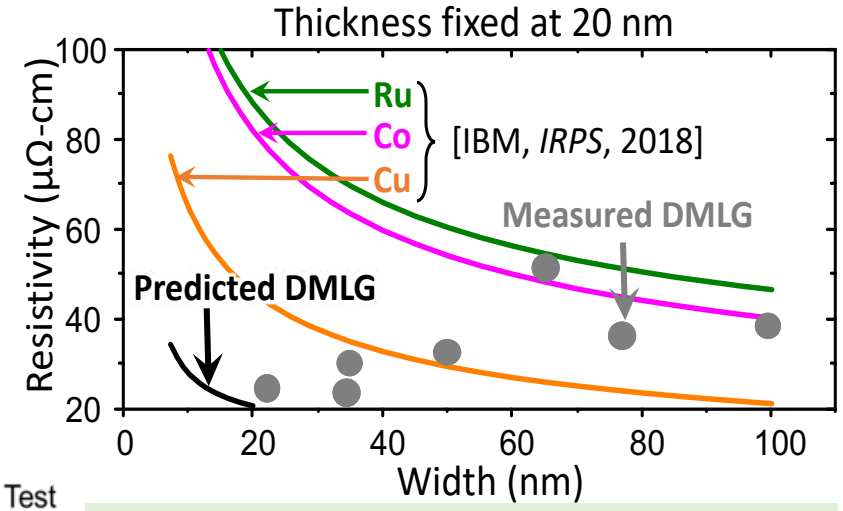
Experimental details regarding the CMOS-compatible MLG growth!!

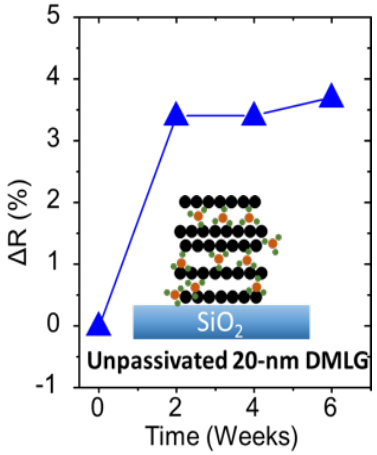
Single Level Doped MLG Interconnects-1

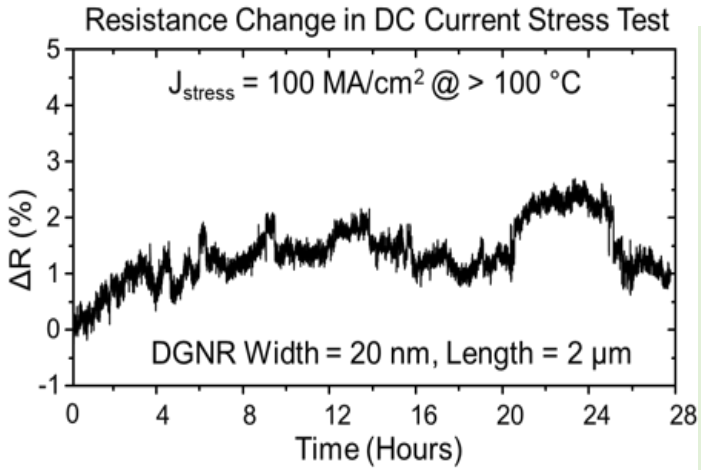


Initial Stack







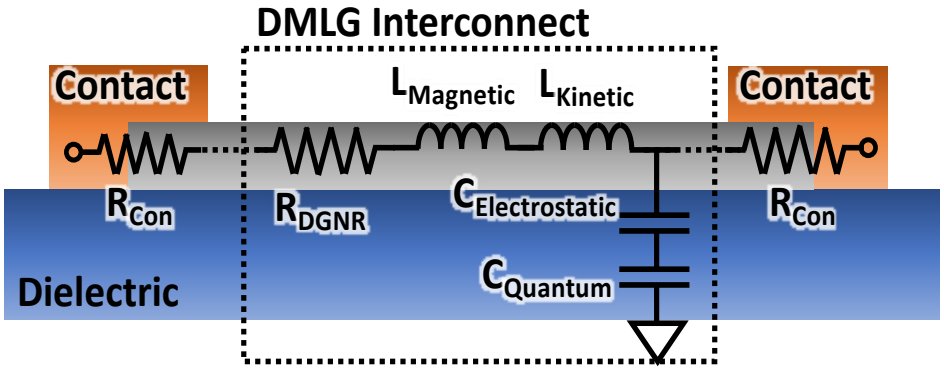


- Subtractive etching based DMLG wires offers ~4x performance improvement as compared to Cu, Co, Ru
- Comparable resistivity to Cu, Co down to sub-20 nm nodes
- > 4 weeks doping stability
- < 2% change in resistance during EM stress tests

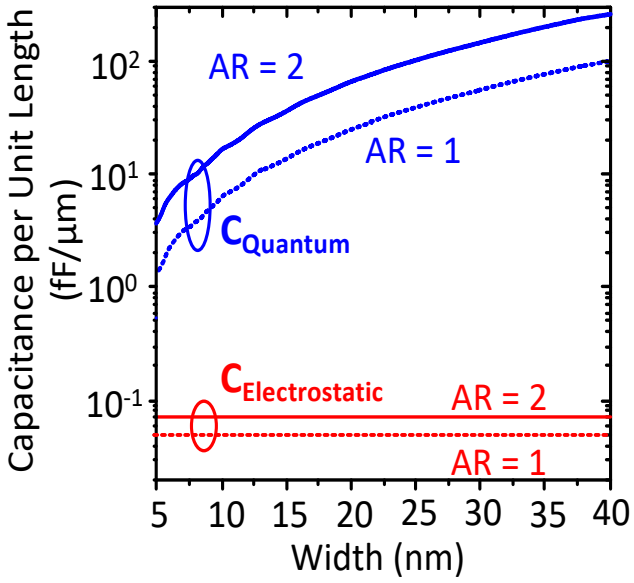
J. Jiang et al., *IRPS*, 2017.

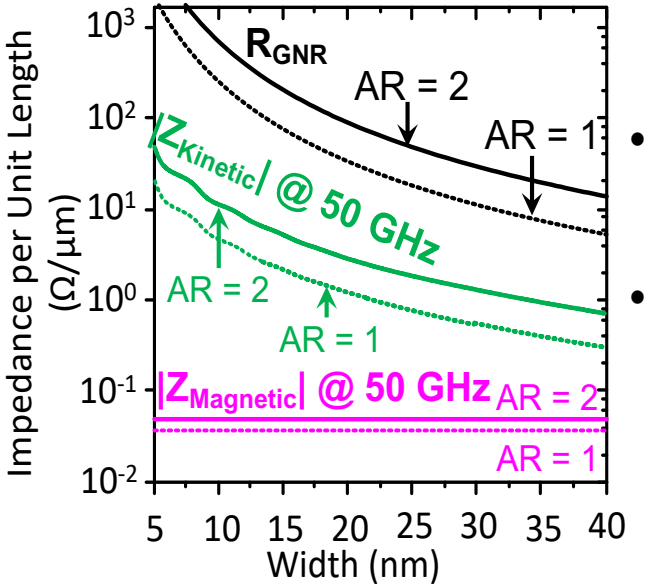
J. Jiang et al., *IEDM*, 2018.

DMLG Modeling for Interconnect Applications



- DMLG distributed RLC model
- Quantum capacitance ($C_{Quantum}$) from limited DOS
- Kinetic inductance ($L_{Kinetic}$) from carrier inertia

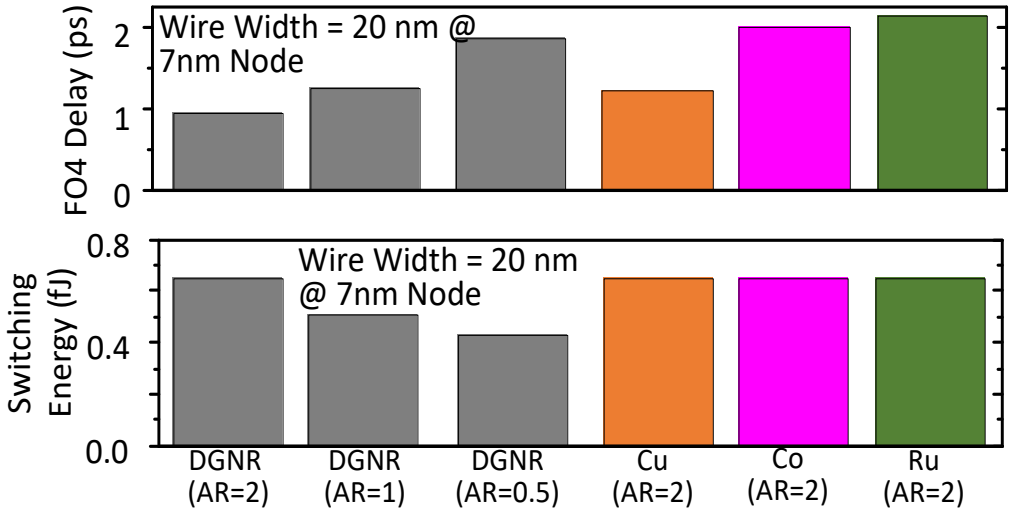




- $C_{Quantum}$, $L_{Magnetic}$ and $L_{Kinetic}$ are negligible at local level
- Distributed RC model is sufficient for DMLG at local level

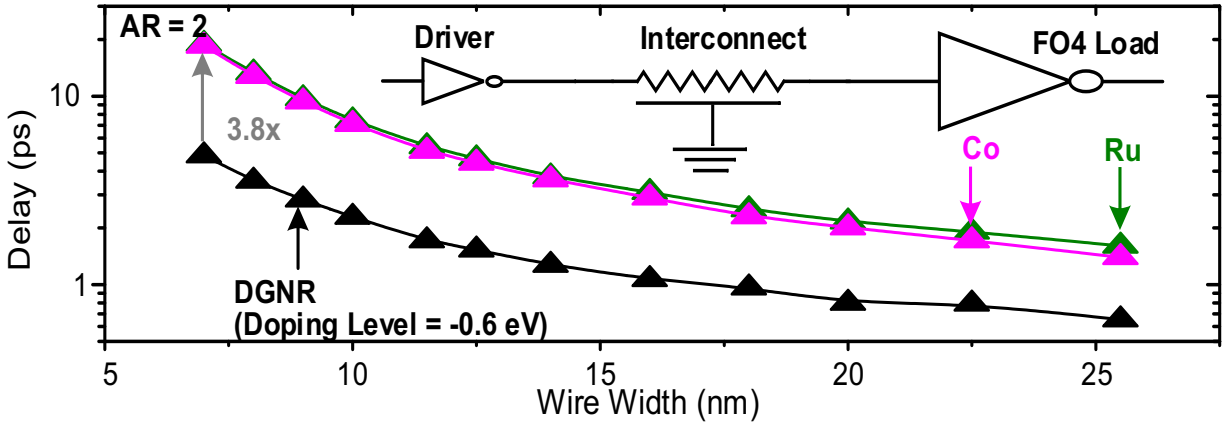
J. Jiang, et al., *NanoHUB*, 2016 (**UCSB**)

Single Level Doped MLG Interconnects-2



- >20% and >50% performance (delay) improvement w.r.t. to Cu and Co, respectively
- >30% energy efficiency improvement, while maintaining same performance as Co

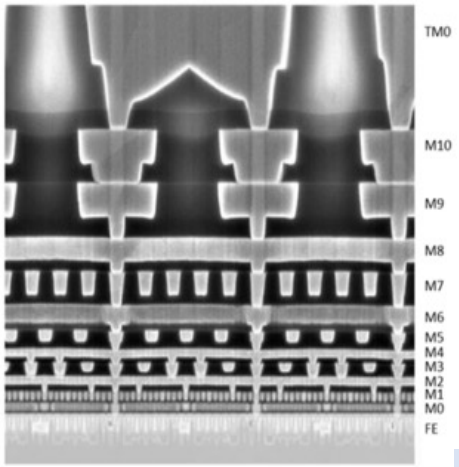
4x performance improvement w.r.t. Co and Ru if max. DGNR doping level is achieved



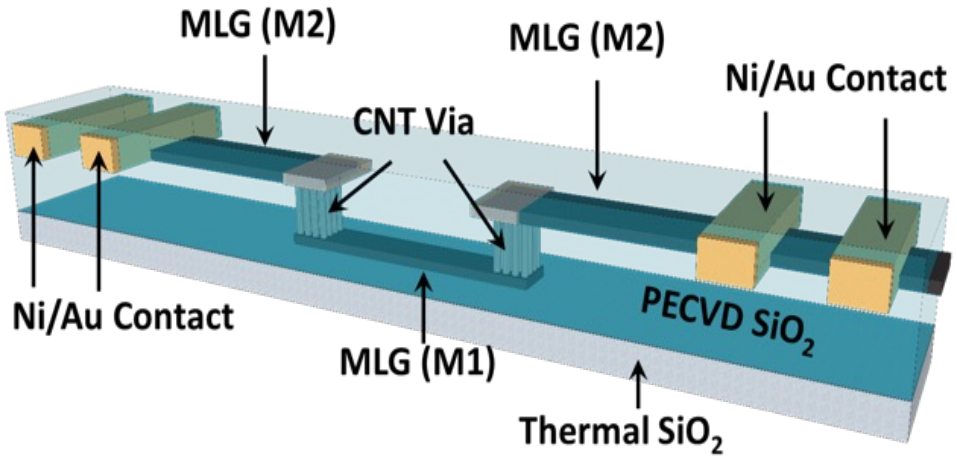
J. Jiang et al., *IEDM*, 2018.

Multilevel MLG Scheme: Toward CMOS-Compatible Carbon Interconnect Process

- Current BEOL technology consists of multiple levels of wires and *vias*
- Need to evaluate the prospects of an MLG-based BEOL-technology



C. Auth, et al., *IEDM*, 2017.



- **First demonstration** of MLG wire and CNT via integration in a multilevel interconnect test structure
- Growth of CNTs requires temperatures > 650 ^{0}C and requires transfer (**not BEOL-compatible**)

J. Jiang et al., *IEDM*, 2017.

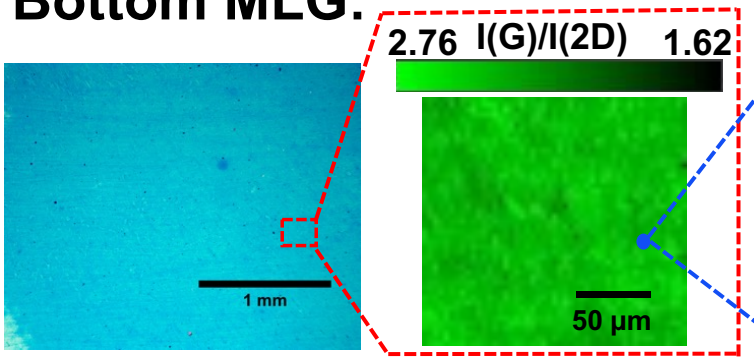
Metallization Requirements [A. J. Learn, *JECS*, 1976]:

1. Compatible deposition techniques
2. Good adherence to di-electrics
3. Low electrical resistivity and contact resistance
4. **Multi-level capability**

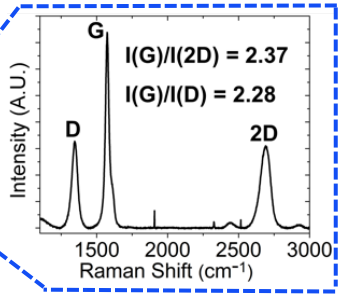
Need to demonstrate the CMOS-compatible MLG growth approach on multiple levels!!

Multi-level MLG Characterization

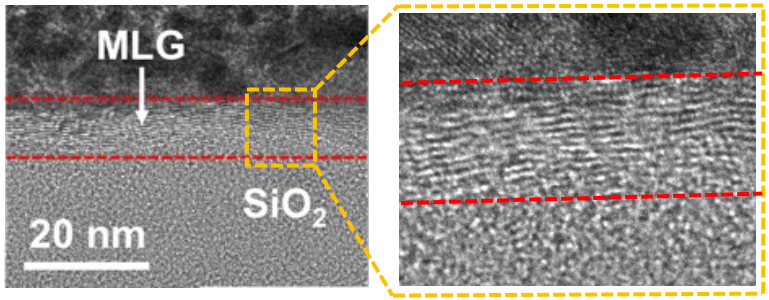
Bottom MLG:



Optical image | Raman map

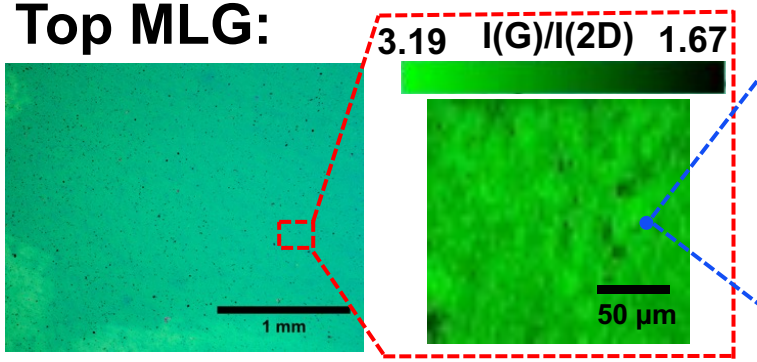


Raman spectra

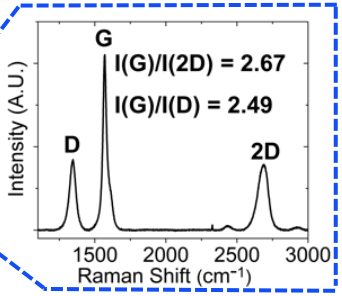


TEM image

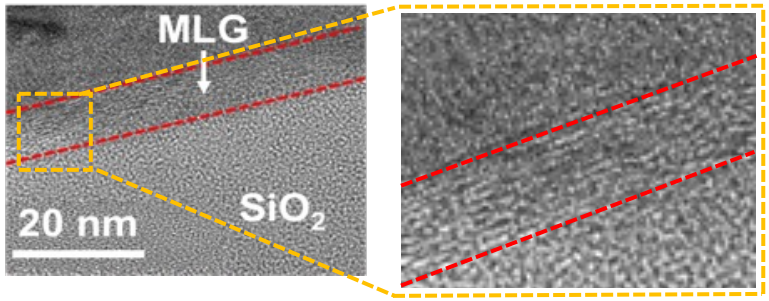
Top MLG:



Optical image | Raman map



Raman spectra



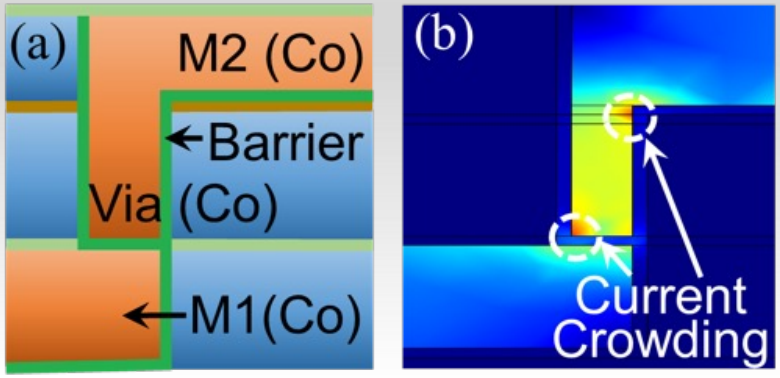
TEM image

K. Agashiwala et al., IEDM, 2020.

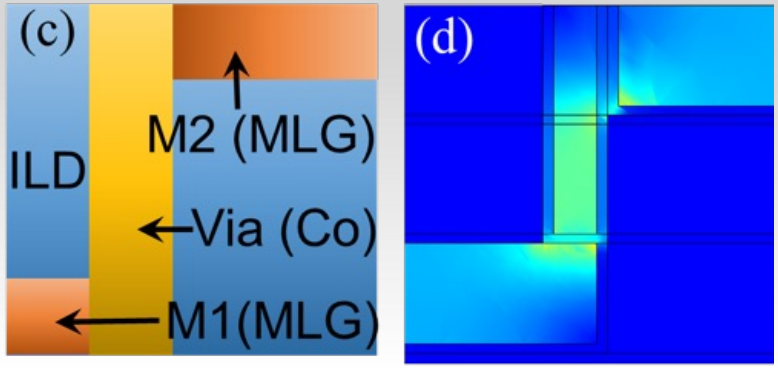
Both top and bottom MLG show identical characteristics

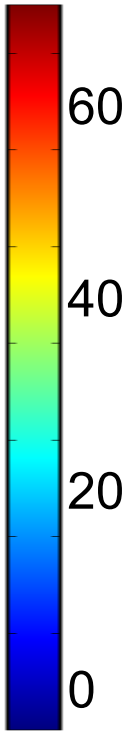
Multi-level MLG Benefits- 1

Dual Damascene Via

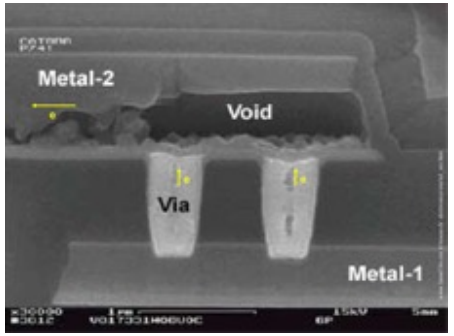


Proposed SE-Compatible Via





Voids Formation from Current Crowding



J. Lienig et al., *ISPD Keynote*, 2006.

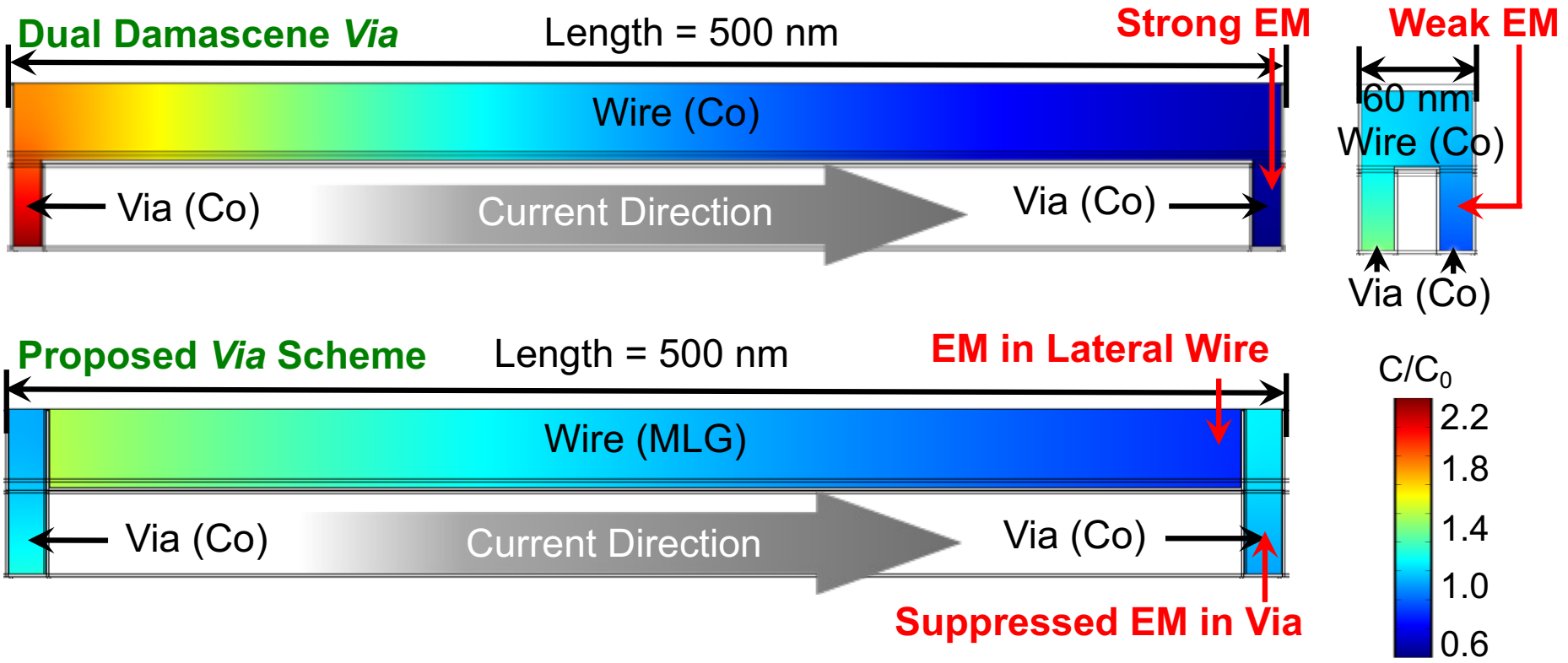
Current redistribution because of edge-contact resistance between MLG and metal *via*

K. Agashiwala et al., TED, 2021.

Multi-level MLG interconnects can help reduce current crowding!!

Multi-level MLG Benefits- 2

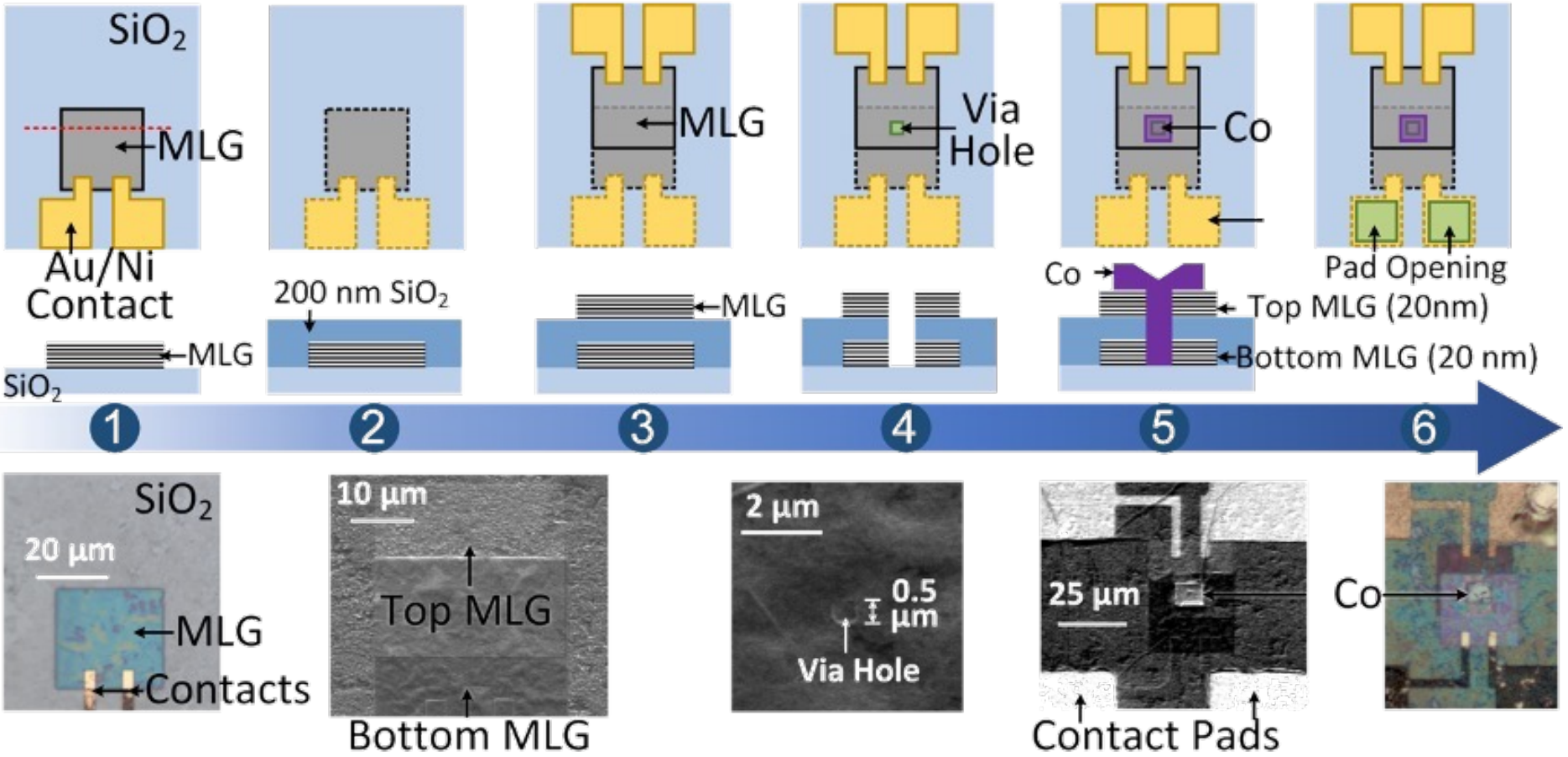
Atomic Concentrations from Self-Heating and EM Simulations



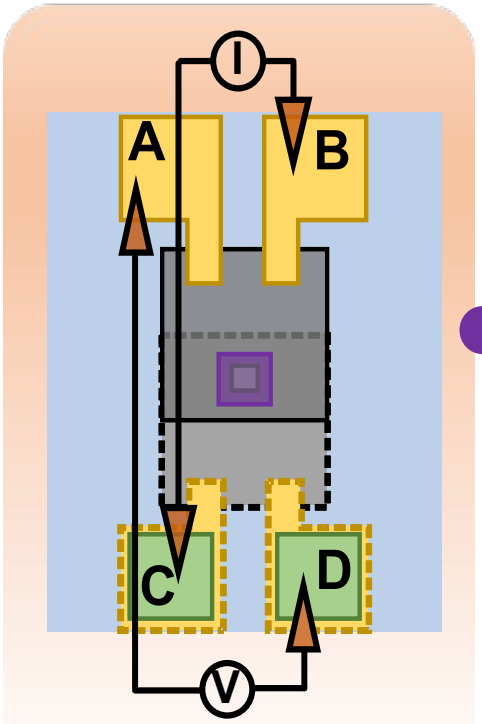
K. Agashiwala et al., TED, 2021.

Multi-level MLG interconnects can help alleviate EM!!

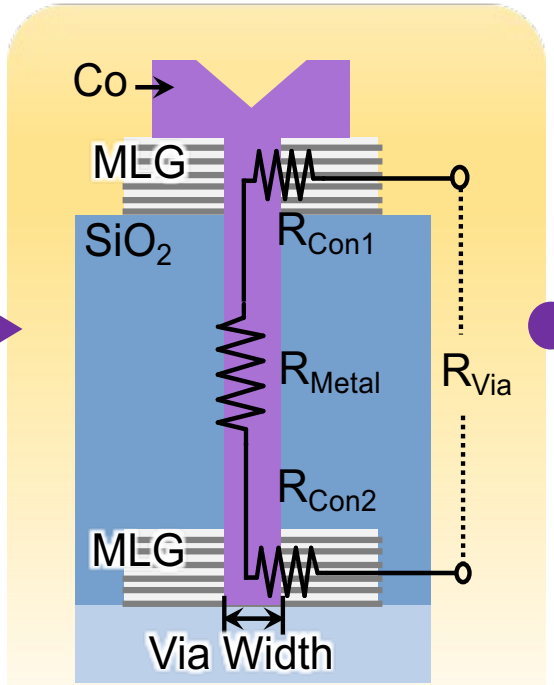
Fabrication of Multi-level MLG Interconnects



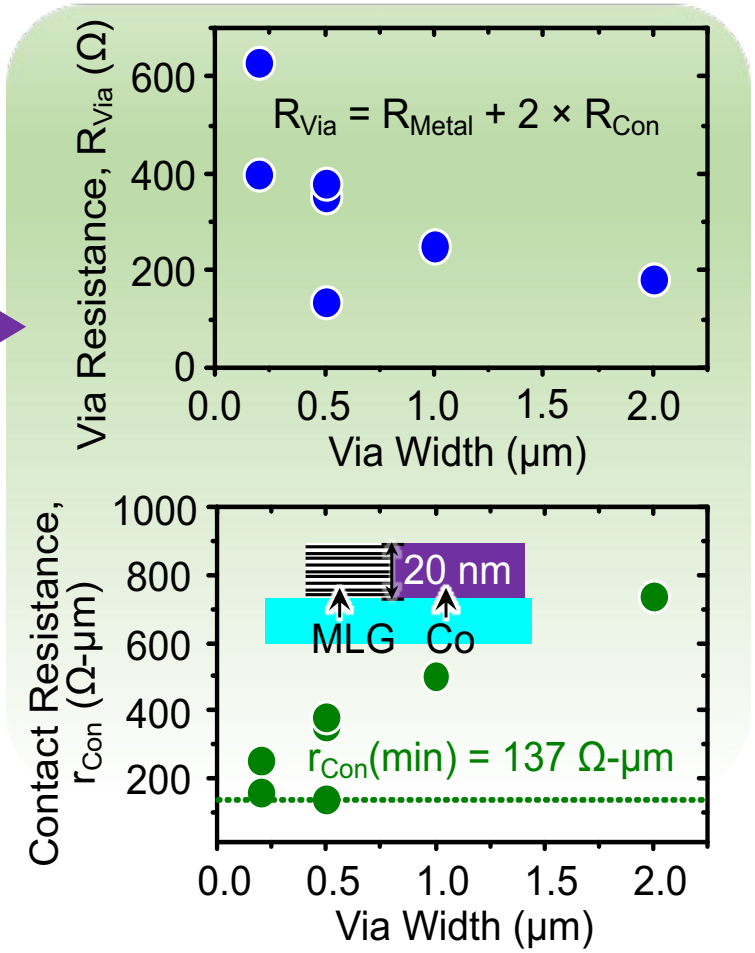
Electrical Characterization



- 4-probe measurement
- MLG resistance << Via resistance

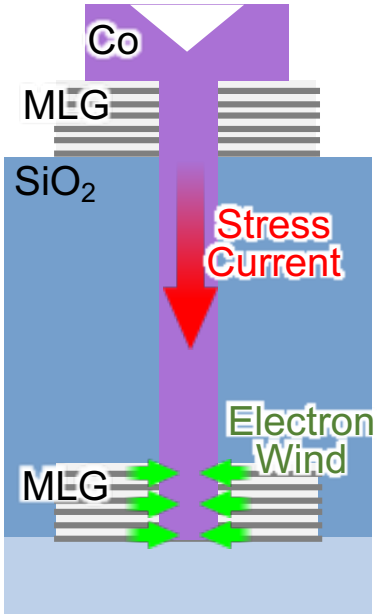


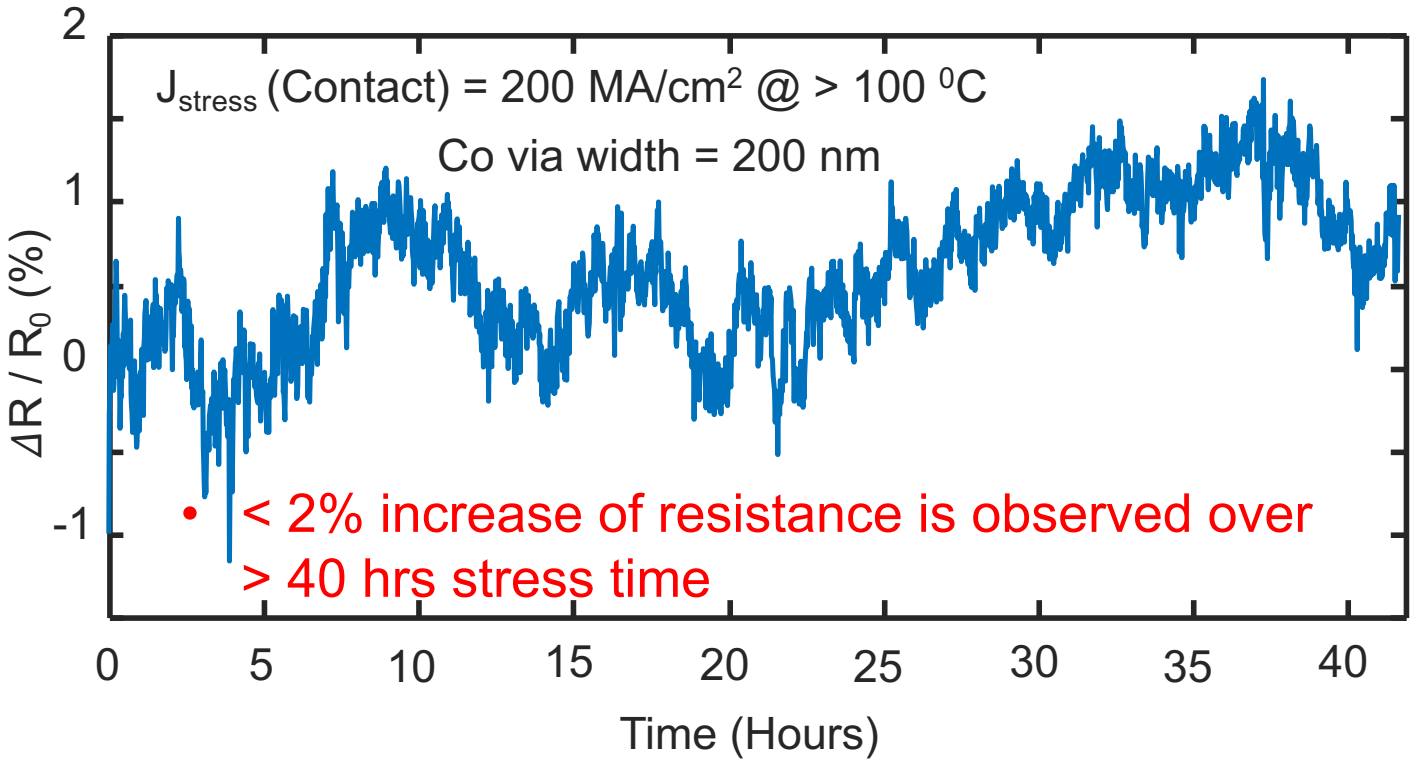
- $R_{Con1} = R_{Con2}$
- $R_{Via} = R_{Con1} + R_{Metal} + R_{Con2}$
  $= R_{Metal} + 2 \times R_{Con}$



K. Agashiwala et al., IEDM, 2020.

Reliability Characterization

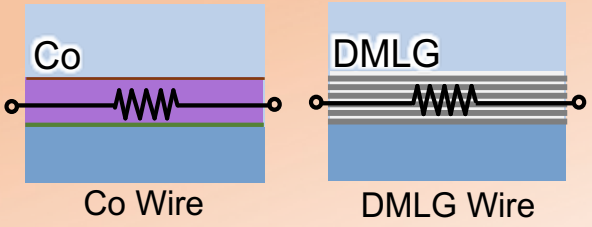


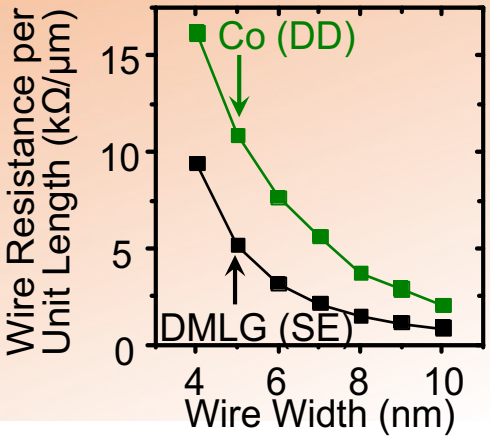


K. Agashiwala et al., IEDM, 2020.

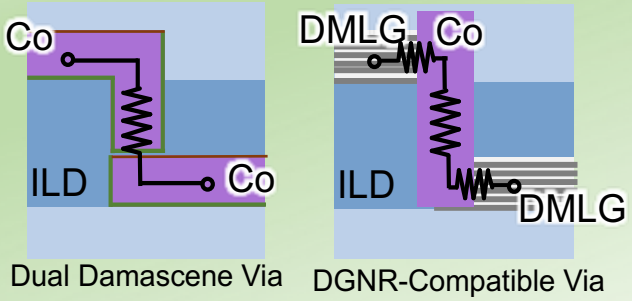
Performance Projections

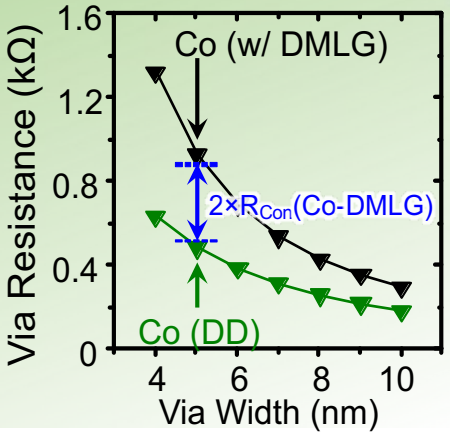
Wire Resistance



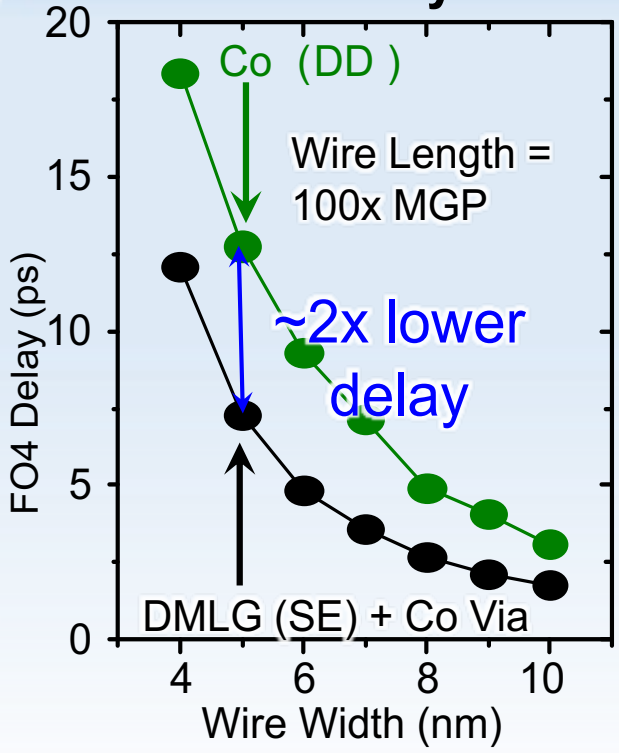


Via Resistance





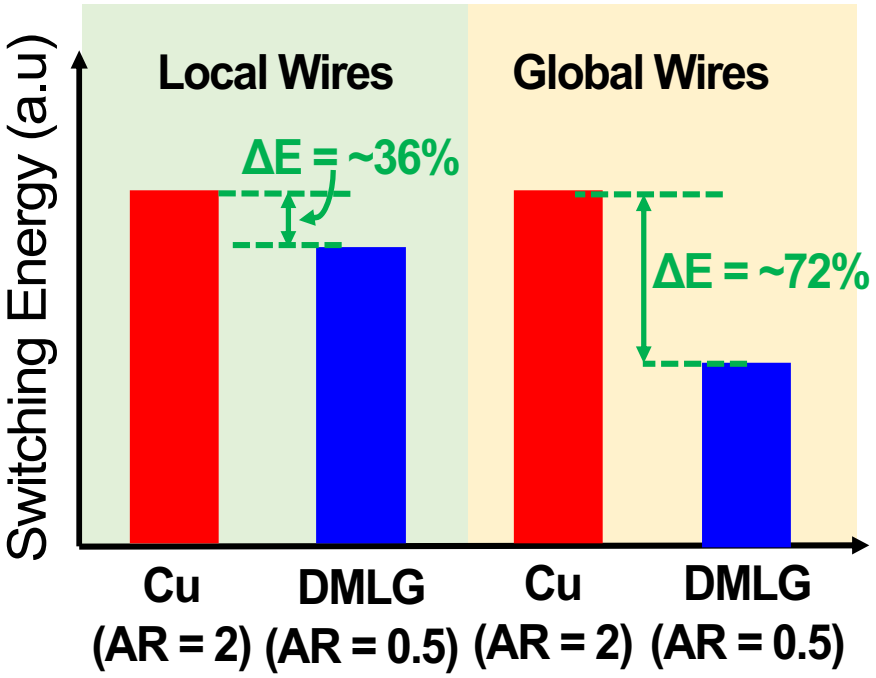
FO4 delay

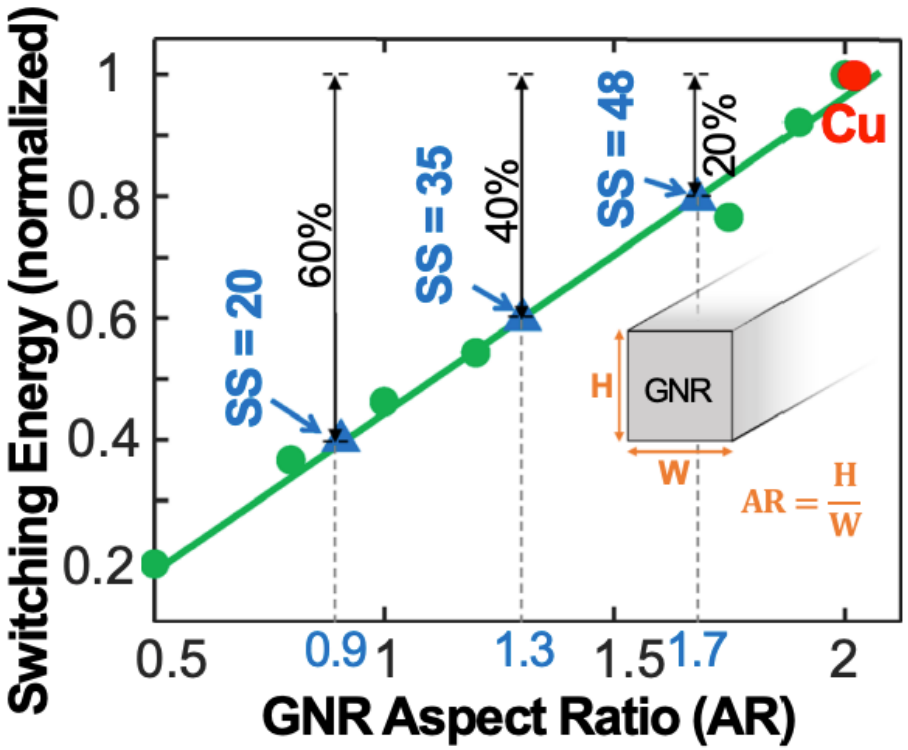


Wire thickness = 20 nm

K. Agashiwala et al., IEDM, 2020.

Comparison of MLG with a steep slope device



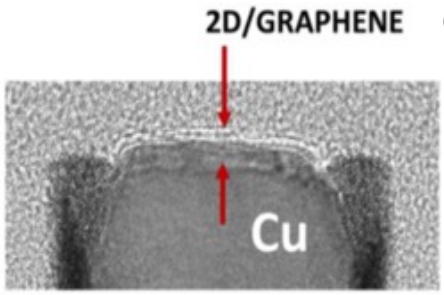


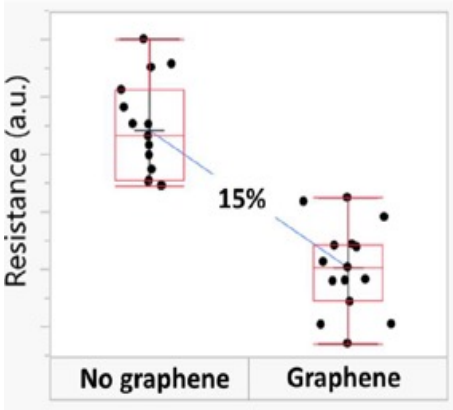
A. Pal, K. Agashiwala et al., MRS Bulletin, 2021.

K. Agashiwala et al., IEDM, 2020.

One alternative to reducing the overall switching energy is to use MLG wires instead of steep slope devices (like TFETs) !!

Graphene as Capping on Cu





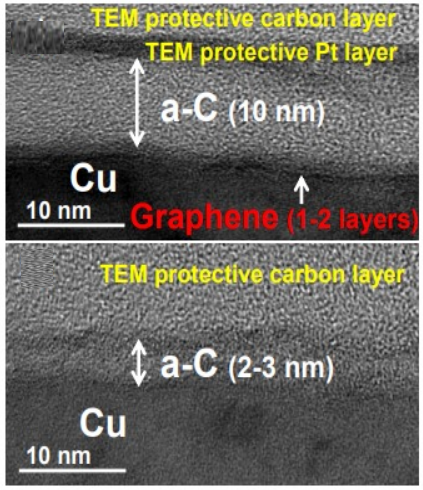
~15 % reduction in resistance due to Graphene capping

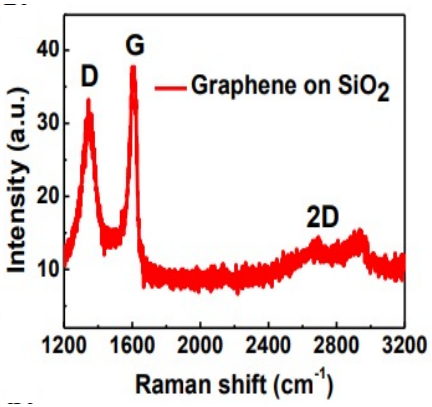
R. Chau, *IEDM*, 2019 (**Intel**).

M. Kobrinsky, *VLSI Symp.*, short course, 2020 (**Intel**).

Optimal graphene diffusion/barrier layer requirements:

- Low temperature growth (< 500^0 C)
- Controllable high quality few-layer graphene

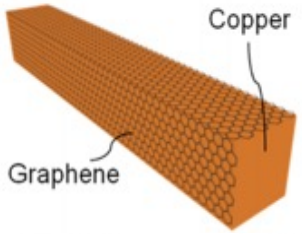


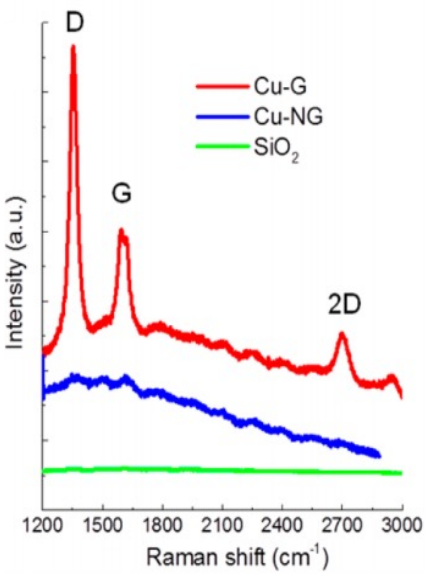


10 nm a-C by-product on top of graphene

L. Li et al., *IEDM*, 2016.

Need for a clean approach to grow MLG on Cu at low-temperatures!!

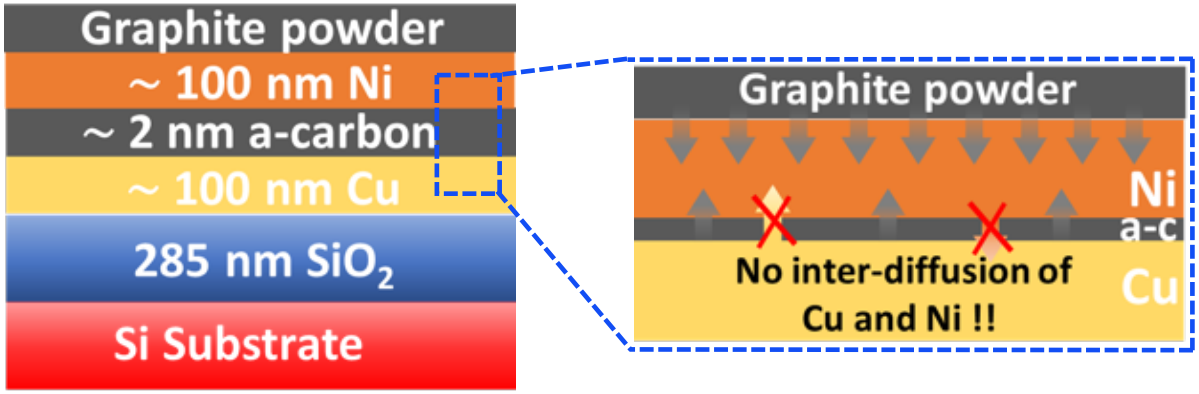




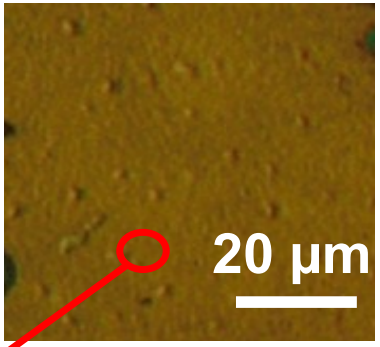
~650 ^{0}C growth temperature
High D/G ratio

R. Mehta et al., *Nano Letters*, 2015.

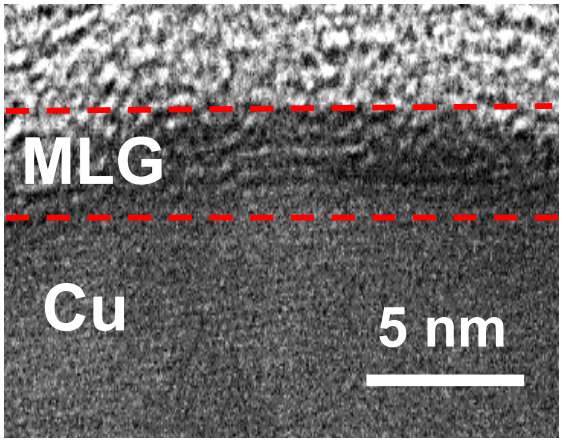
CMOS-Compatible MLG Growth on Cu



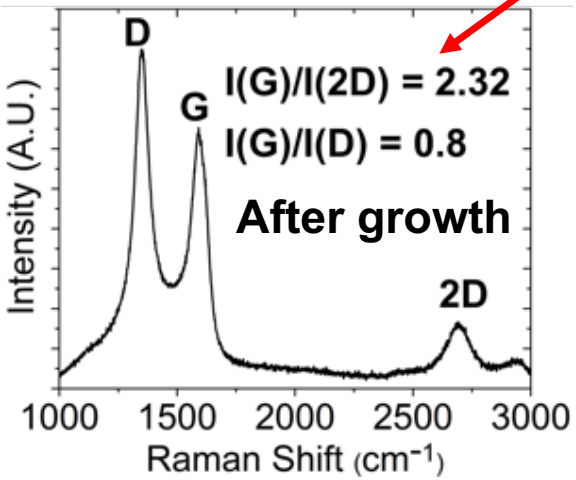
Initial Stack

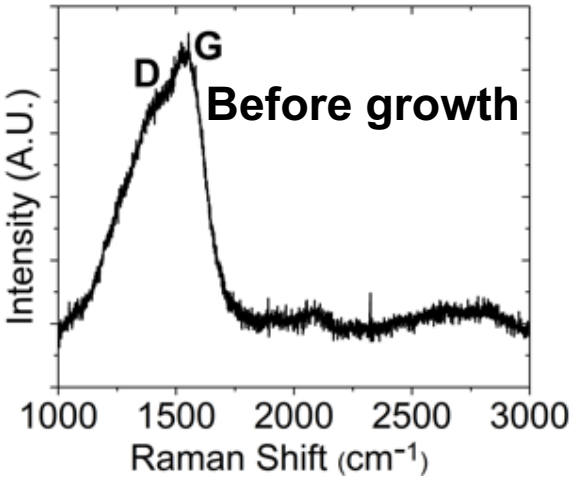


Optical image



TEM image

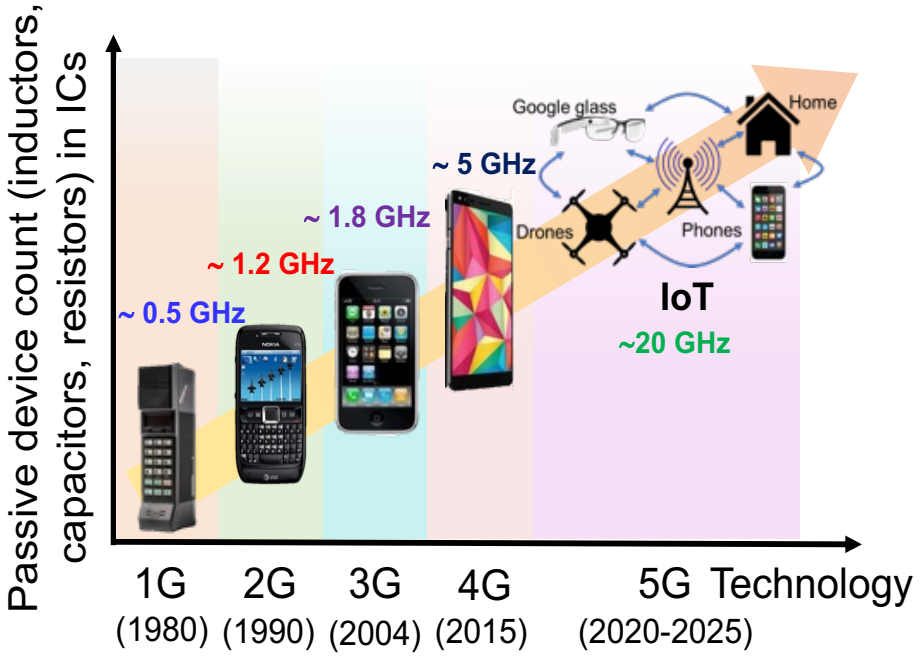


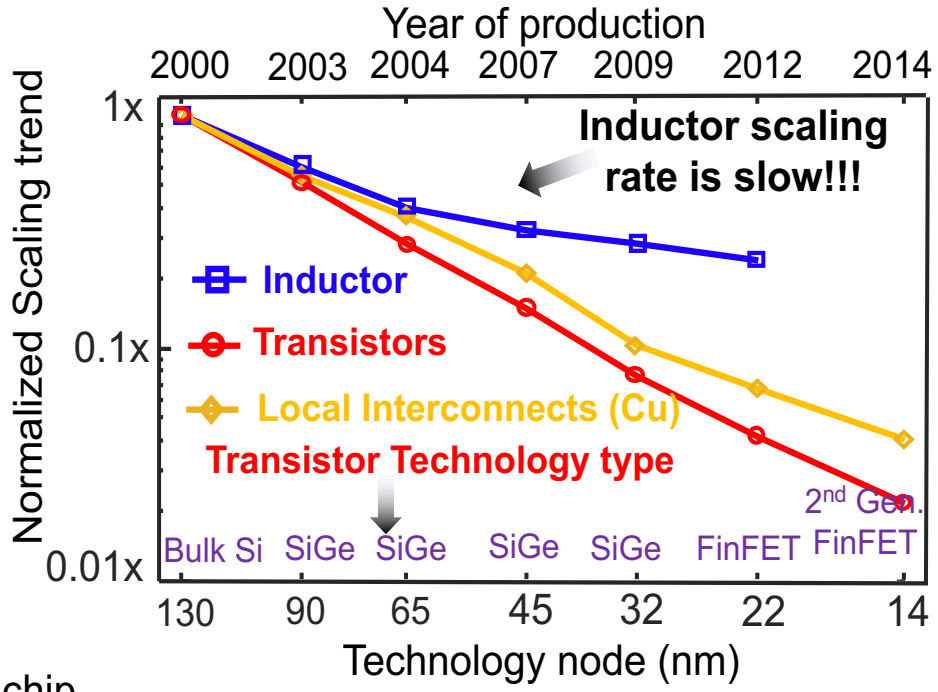


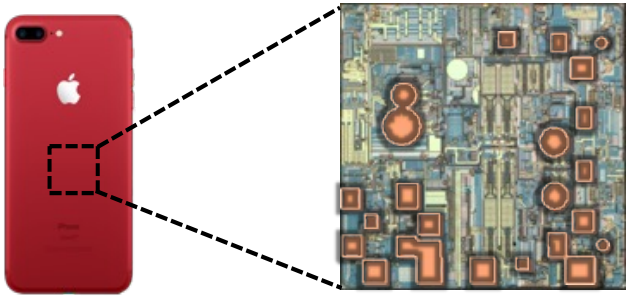
Raman Spectra

K. Agashiwala et al., IEDM, 2020.

Graphene based inductors: RF-IC Scaling and Evolution







Apple iPhone7 plus

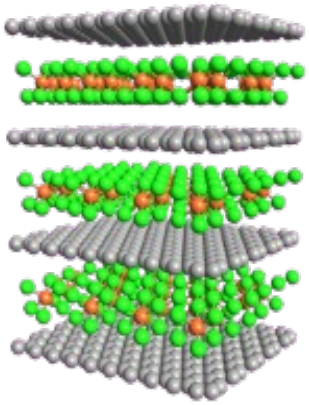
Qualcomm RFIC (iPhone 7 plus)

up to 50% chip area occupied by inductors

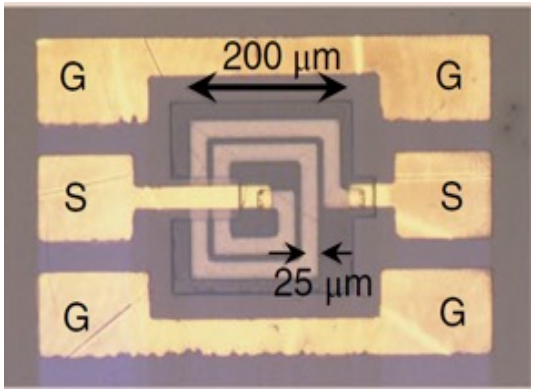
Inductor is a major bottleneck for RF-IC (IoT) miniaturization !!!

K. Agashiwala et al., IEDM, 2018.

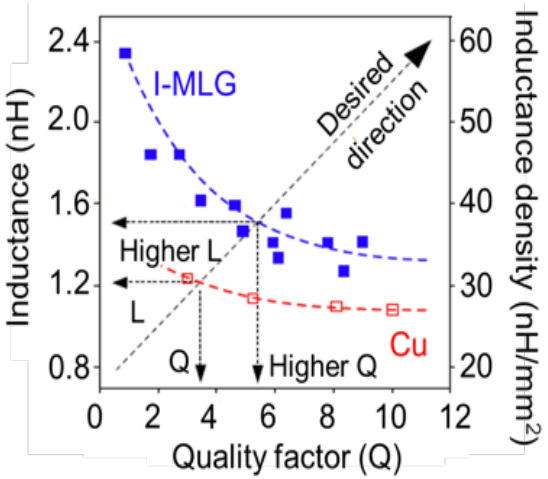
Inductor Scaling using I-MLG: "Kinetic Inductor"



Intercalated MLG



Schematic of MLG inductor



- Intercalation of MLG was used to design materials with the **highest inductance density** (1.5x) ever[1]

1. J. Kang, et al., *Nature Electronics, 2018 (**UCSB**).*

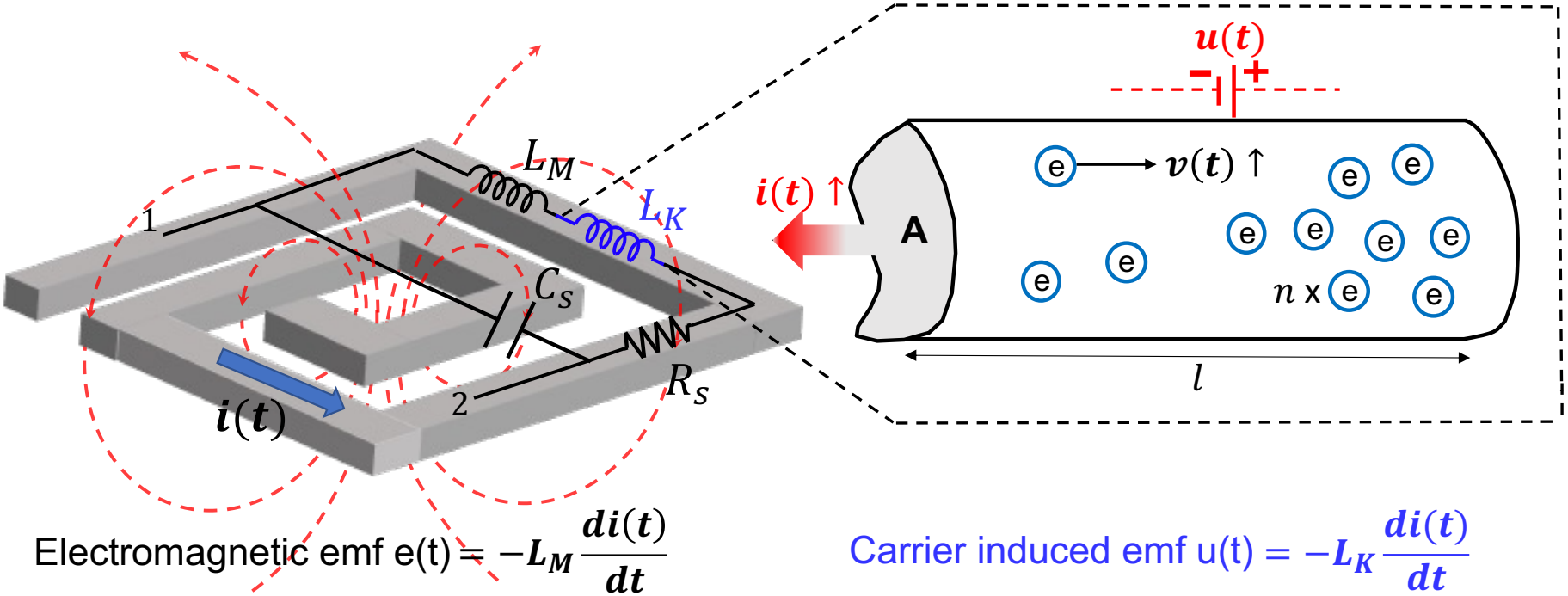
- Realization of Intercalated MLG based spiral inductors with a **high Q** (up to 12) for 5G frequency range[1] (>20 GHz)
- Kinetic Inductance: well known concept in condensed matter physics[2,3] (cryogenic temp. detectors)

2. P. K. Day, et al., *Nature, 2003* 3. R. Meservey, et al., *Journal of App. Phy., 1959*

K. Agashiwala et al., IEDM, 2018.

Difference between Magnetic and Kinetic Inductance

Difference between Magnetic and Kinetic Inductance



Electromagnetic emf $e(t) = -L_M \frac{di(t)}{dt}$

Magnetic Inductance (L_M)

- $L_M = L_{self} + L_{mutual}$
- Depends on the geometry of the system

Carrier induced emf $u(t) = -L_K \frac{di(t)}{dt}$

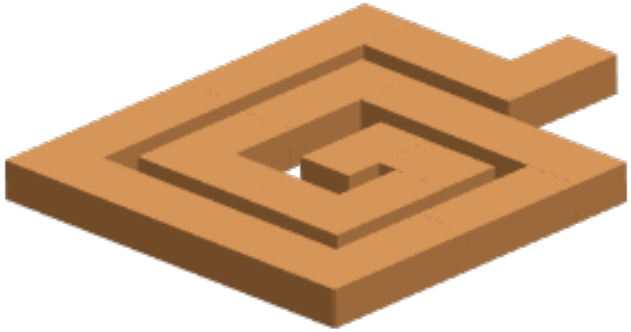
Kinetic Inductance (L_K)

- Intrinsic property of every material
- Kinetic inertia of the carriers
- Appears in series with L_M

K. Agashiwala et al., IEDM, 2018.

How Good can I-MLG Inductors be ?

2-turn spiral inductor



Outer diameter = 200 μm, Thickness = 1 μm,
Width = 10 μm, Inter-turn spacing = 10 μm

Magnetic Inductance (L_M) **~ 1.2 nH** (HFSS)

(Equivalent for both Cu and I-MLG inductors)

Kinetic Inductance (Cu) ~ **0.16 nH**

Kinetic Inductance (I-MLG) ~ **4.12 nH**

Up to 3x improvement in total inductance density ($L_M + L_K$) for I-MLG as compared to Cu !!

K. Agashiwala et al., IEDM, 2018.